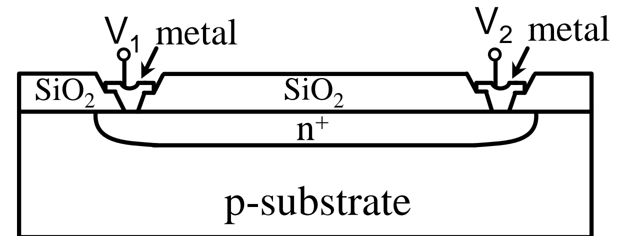
Semiconductor Devices and Models

Semiconductor Devices and Models

- Resistor
- Capacitor
- Diode
- Bipolar Transistor
- MOSFET
- SPICE Model
- Appendix

Resistors

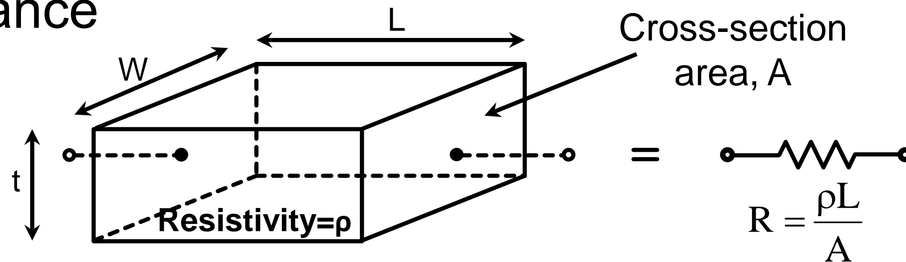
- Material
  - Diffusion layers: e.g. n+, p+, well
  - Conductors: e.g. polysilicon, …



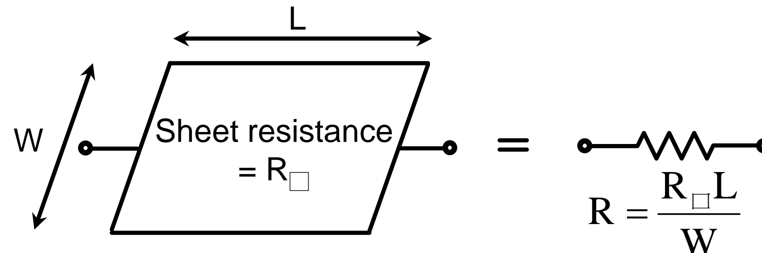
- Resistance calculation
  - $R = \rho L/A = \rho L/tW = R_{\square} L/W$

    ρ is resistivity

    $R_{\square} = \rho/t$ is sheet resistance

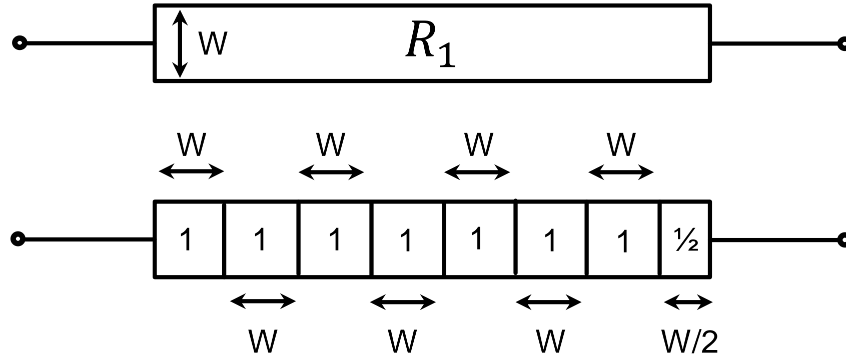


- Sheet resistance ($R_{\square}$)

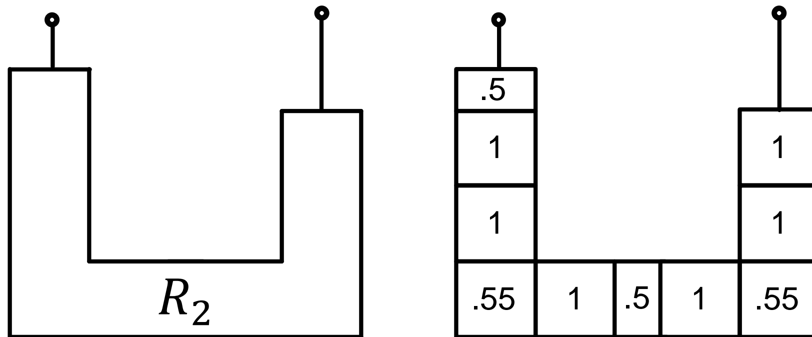


Resistors (Cont.)

- Graphical calculations from sheet resistance



$R_1 = 7.5R_{\square}$

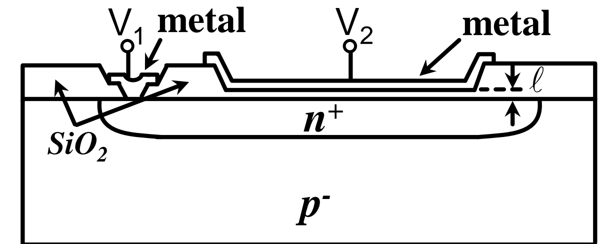


$R_2 = 8.1R_{\square}$

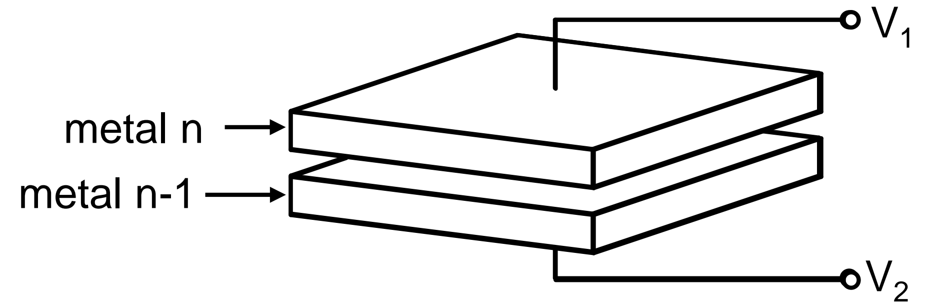
- VC (voltage coefficient) and TC (temperature coefficient) of R (or C)
  → Nonlinearity → THD

Capacitors

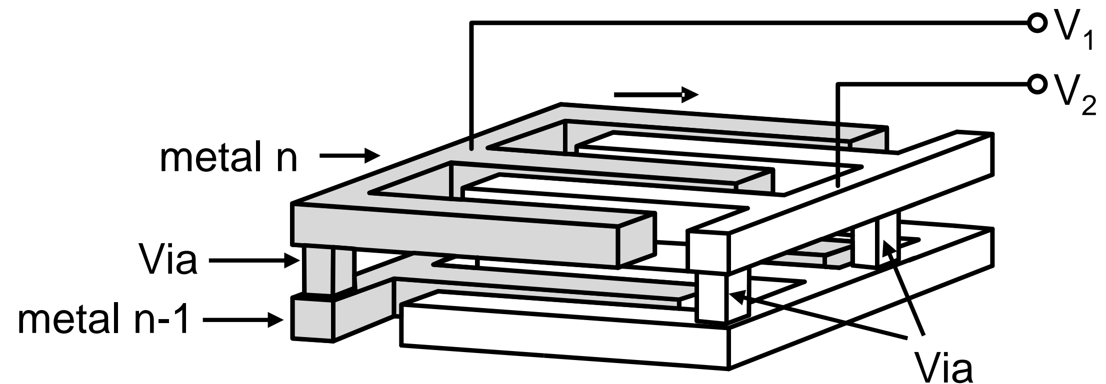
- Metal- or polysilicon- over-diffusion
  - Capacitance is voltage dependent



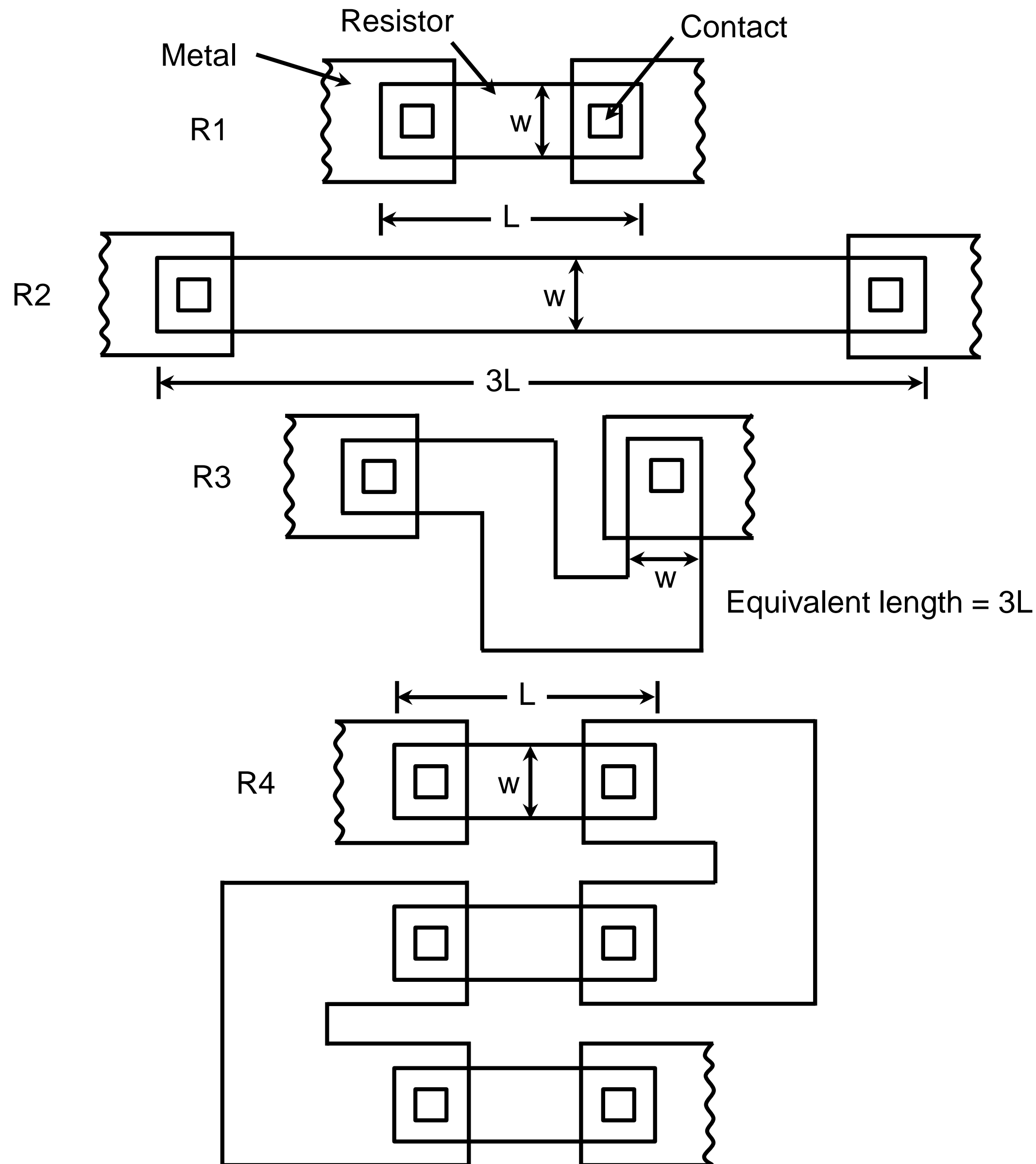
- Metal-Insulator-metal (MIM)
  - High linearity



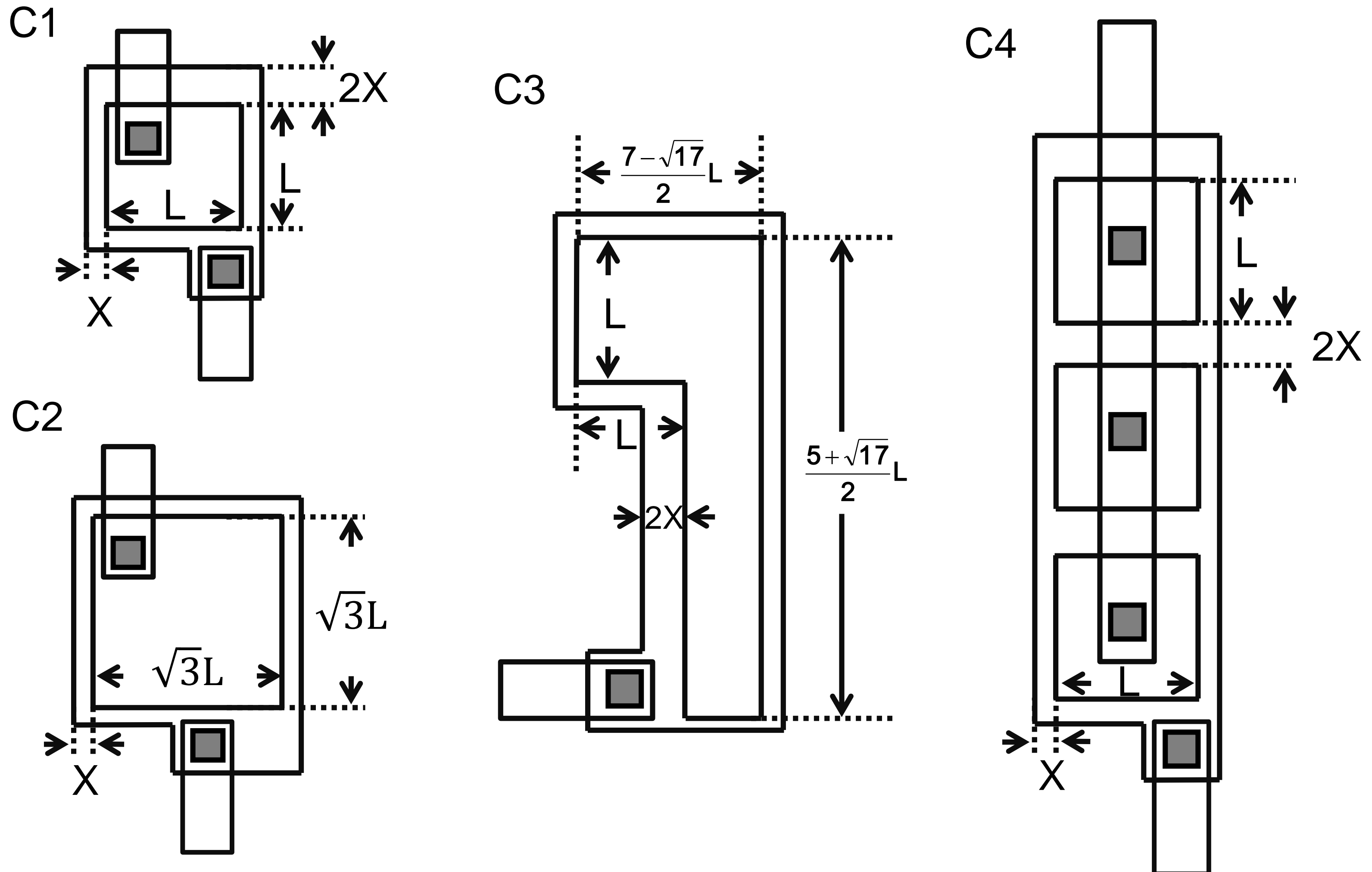
- Inter-metal and intra-metal
  - Inter: Different layer
  - Intra: Same layer



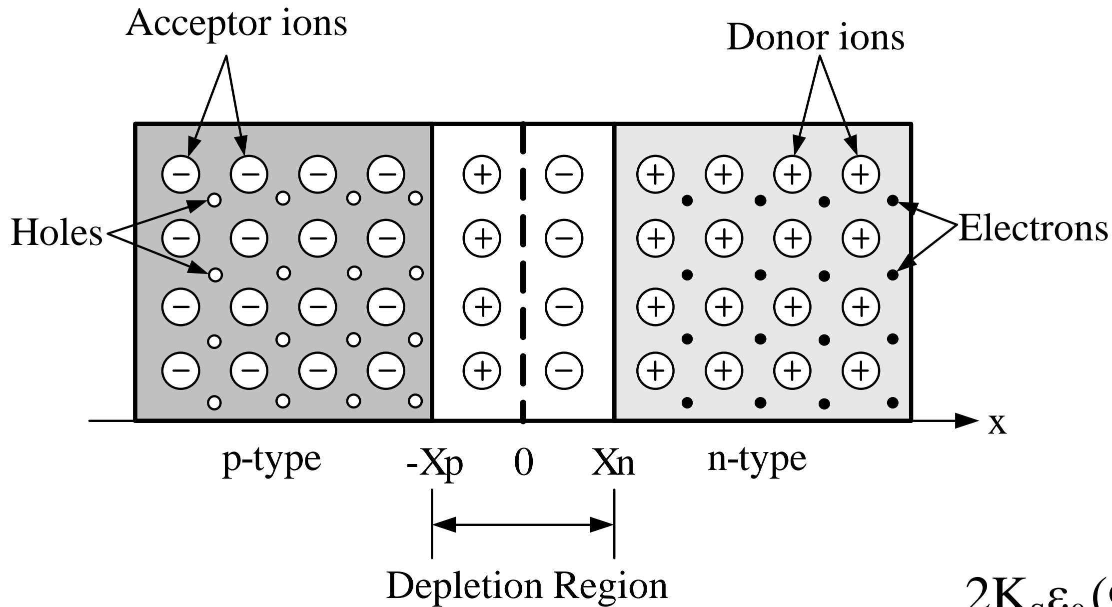
Resister Ratio-matching Considerations

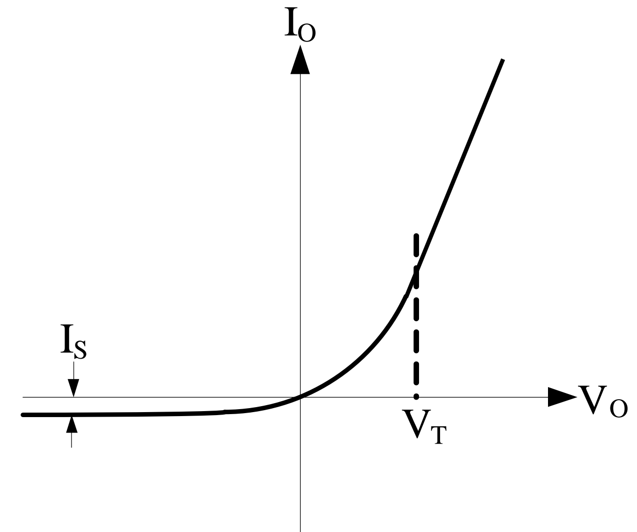


Capacitor Ratio-matching Considerations



Diode





$$I = I_S(\exp^{\frac{V}{V_T}} - 1)$$

where $V_T = \dfrac{kT}{q}$

$I_S =$ saturation current

$$Xp = [\frac{2K_S\varepsilon_0(\Phi_0 + V_R)}{q}\frac{N_D}{N_A(N_A + N_D)}]^{1/2}$$

$$Xn = [\frac{2K_S\varepsilon_0(\Phi_0 + V_R)}{q}\frac{N_A}{N_D(N_A + N_D)}]^{1/2}$$

K_s : relative permittivity of silicon

ε_0 : vacuum permittivity

Φ_0 : built-in potential

V_R : reverse-bias voltage

Junction Capacitance

- For abrupt junction:

$$Q^+ = Q^- = [2qK_S\varepsilon_0(\Phi_0 + V_R)\frac{N_A N_D}{N_A + N_D}]^{1/2}$$

$$C_j = \frac{dQ^+}{dV_R} = [\frac{qK_S\varepsilon_0}{2(\Phi_0 + V_R)}\frac{N_A N_D}{N_A + N_D}]^{1/2} = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\Phi_0}}}$$, where $C_{j0} = [\frac{qK_s\varepsilon_0}{2\Phi_0}\frac{N_A N_D}{N_A + N_D}]^{1/2}$

- For graded junction

$$Q^+ = Q^- = [2qK_S\varepsilon_0(\Phi_0 + V_R)\frac{N_A N_D}{(N_A + N_D)}]^{1-m_j}$$

$$C_j = \frac{dQ^+}{dV_R} = (1 - m_j)[2qK_S\varepsilon_0\frac{N_A N_D}{N_A + N_D}]^{1-m_j}\frac{1}{(\Phi_0 + V_R)^{m_j}} = \frac{C_{j0}}{(1 + \frac{V_R}{\Phi_0})^{m_j}}$$

where $C_{j0} = (1 - m_j)[2qK_S\varepsilon_0\frac{N_A N_D}{N_A + N_D}]^{1-m_j}\frac{1}{\Phi_0^{m_j}}$

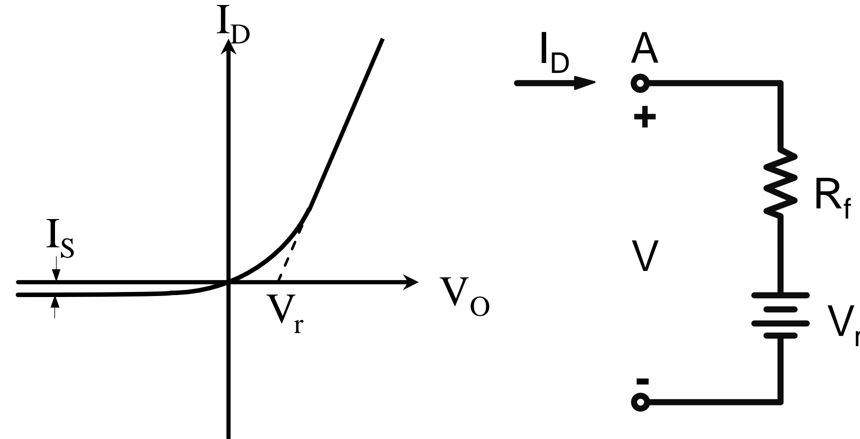
m_j depends on the doping profile

$m_j \approx 1/3$ for a linearly graded junction

Diode Model

- DC Model
  - For $V < V_r$ (off)
  - For $V > V_r$ (on)

$$R_f = \left(\frac{dI}{dV}\right)^{-1} = \frac{V_T}{I_S e^{V_D/V_T}} \approx \frac{V_T}{I_D}$$



- Small Signal Model
  - For forward-biased diode

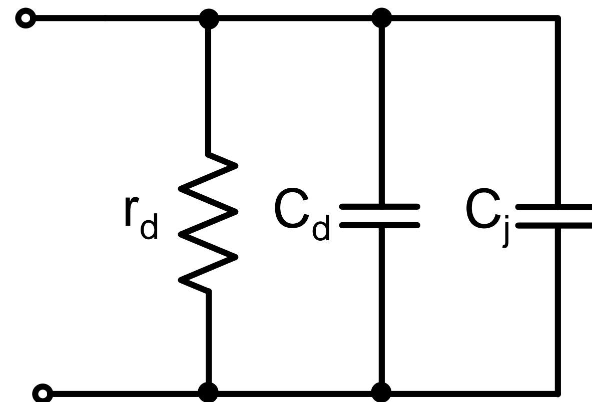
$$r_d \approx \frac{V_T}{I_D}$$

Diffusion capacitance: $C_d \approx \frac{\tau_T}{r_d}$

Junction capacitance: C_j

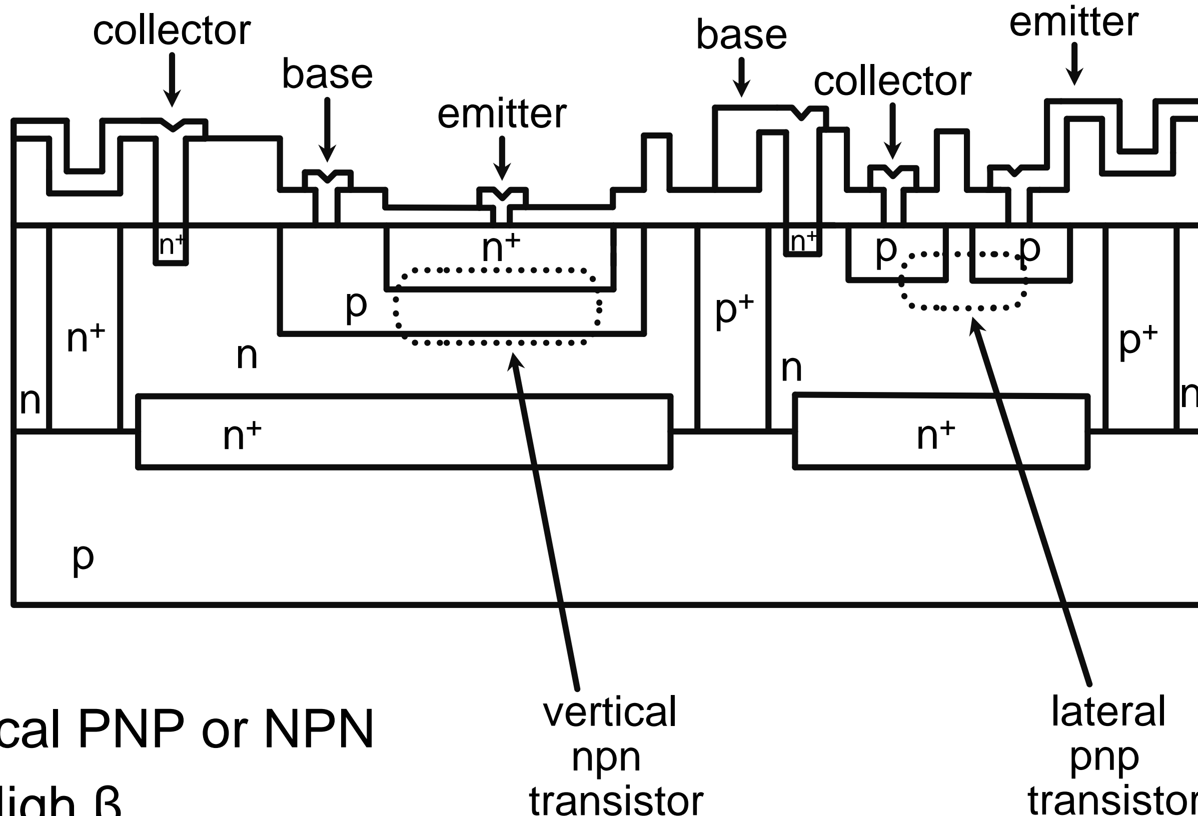
Normally, C_d>>C_j ($C_d \approx 100C_j$)

τ_T : Diode transit time



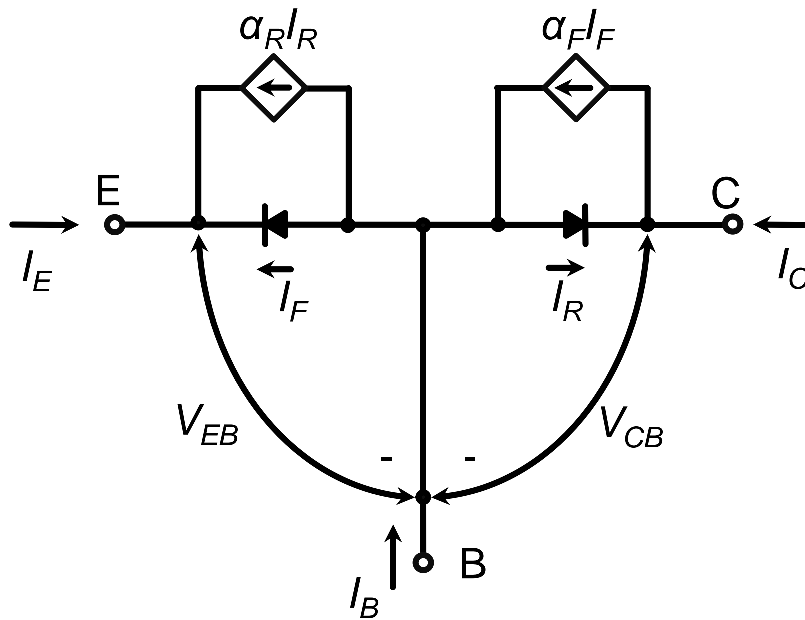
Bipolar Process

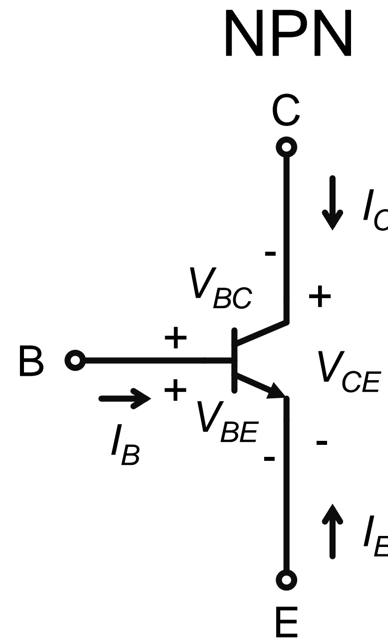
- Vertical and lateral transistor in a bipolar process

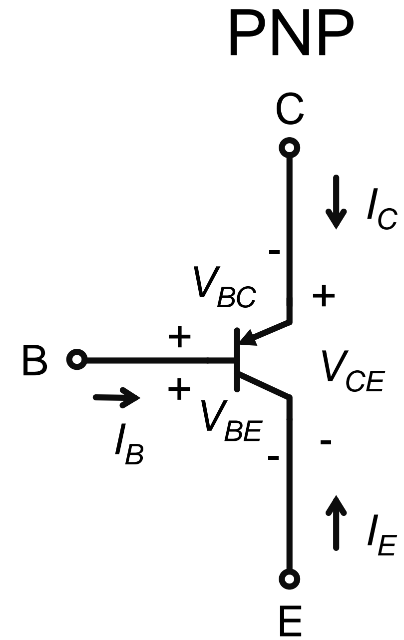


- Vertical PNP or NPN
  - High β
- Lateral PNP or NPN
  - Low β

BJT Model: Ebers-Moll model (DC Model)



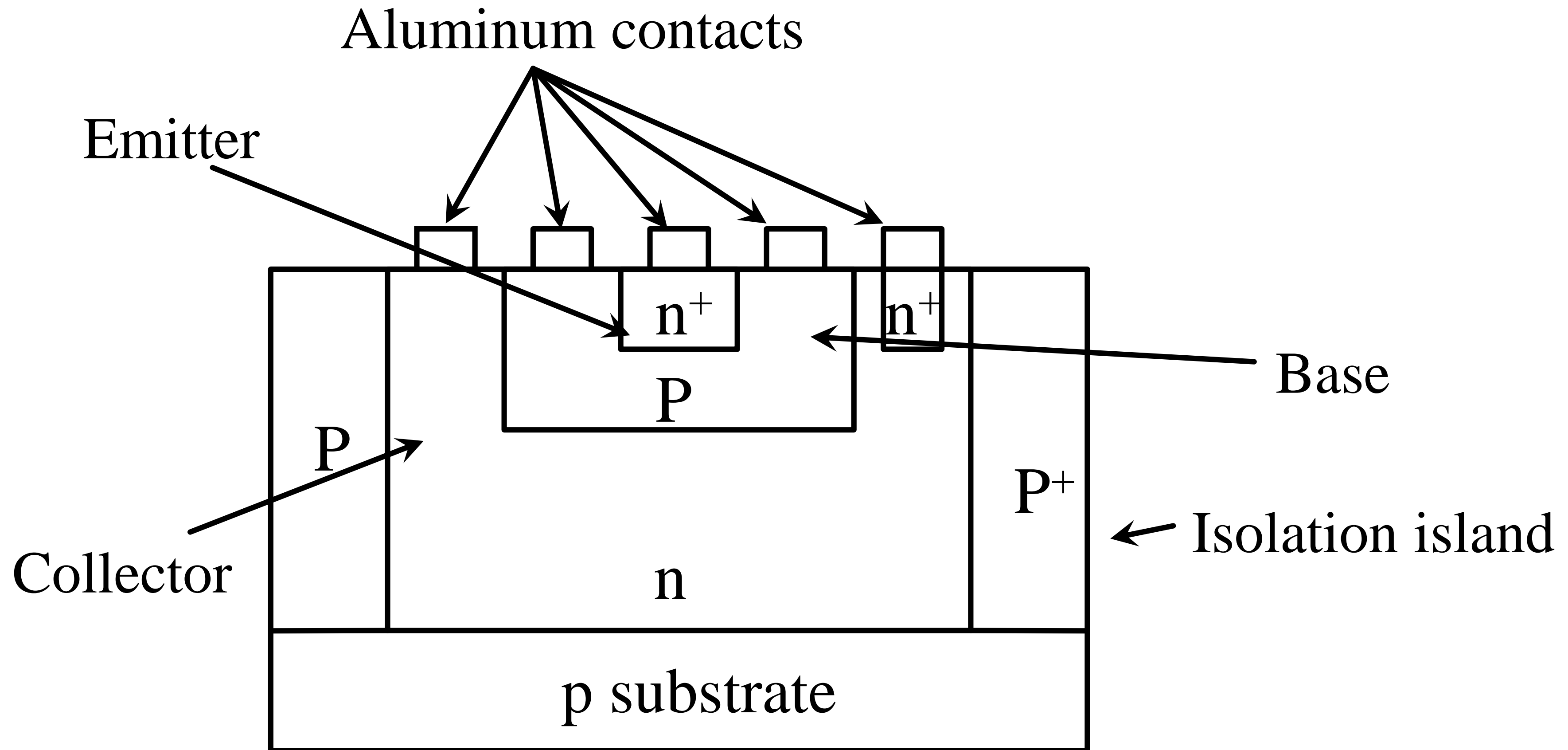




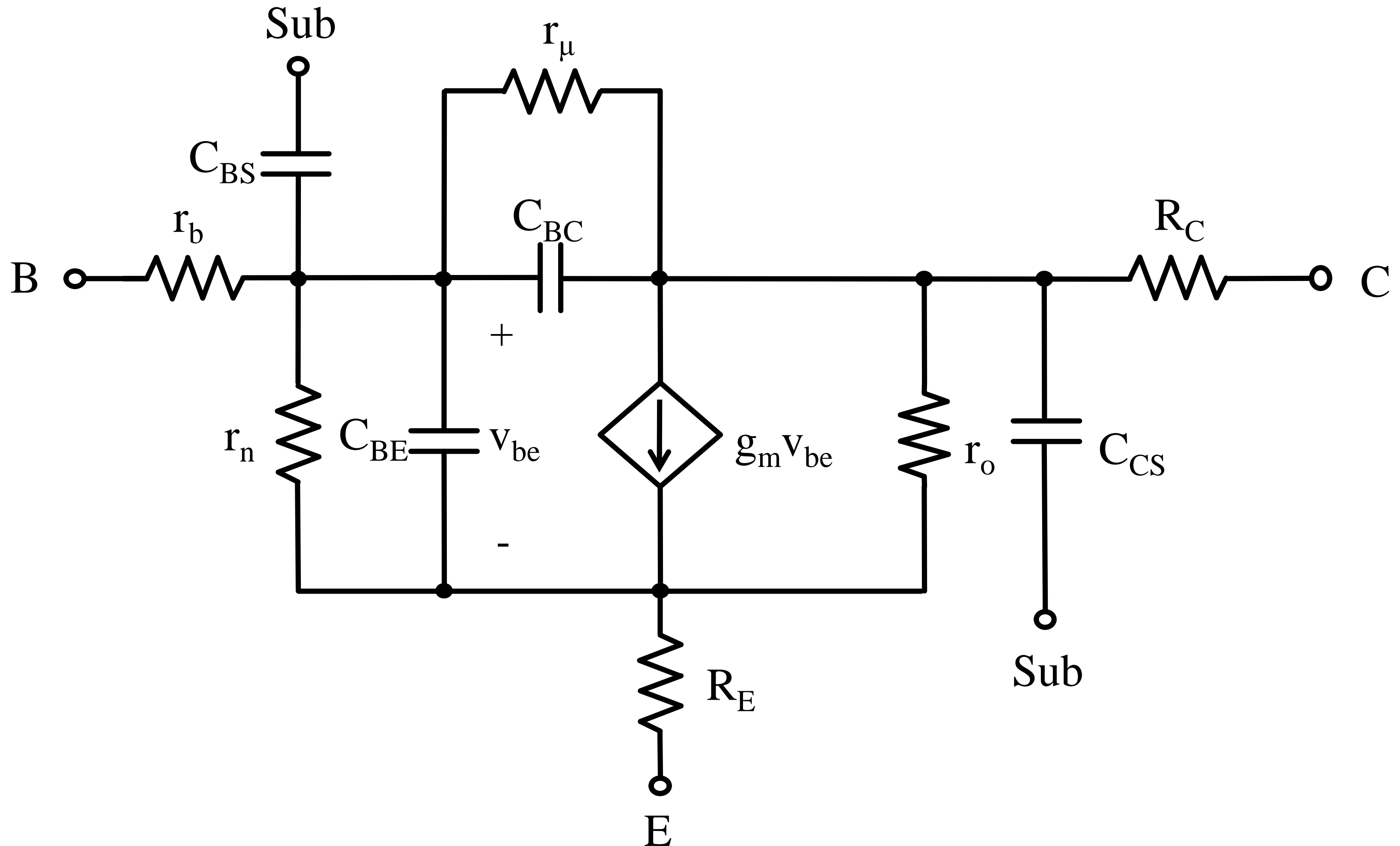
$$I_C = I_S\left[e^{\left(V_{BE}/V_T\right)} - 1\right] - \frac{I_S}{\alpha_R}\left[e^{\left(V_{BC}/V_T\right)} - 1\right]$$

$$I_E = \frac{-I_S}{\alpha_R}\left[e^{\left(V_{BE}/V_T\right)} - 1\right] - I_S\left[e^{\left(V_{BC}/V_T\right)} - 1\right]$$

Small Signal BJT Model



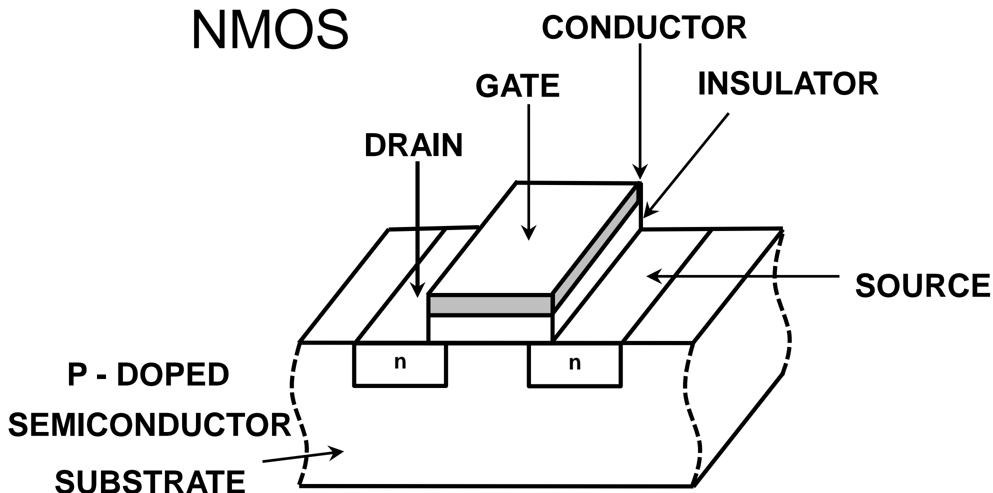
Small Signal BJT Model (Cont.)



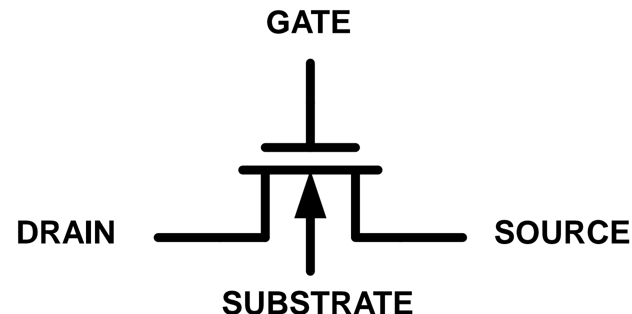
MOS Transistors

- MOS structure

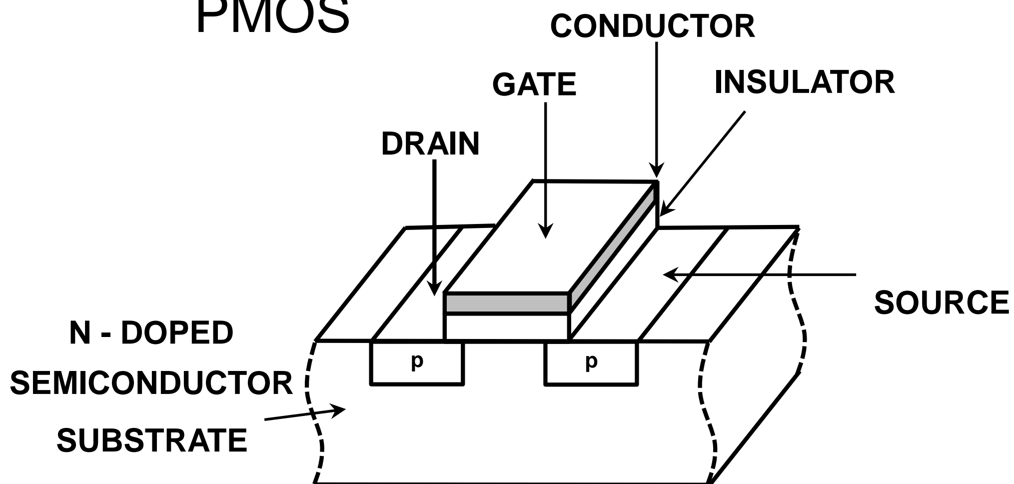
NMOS



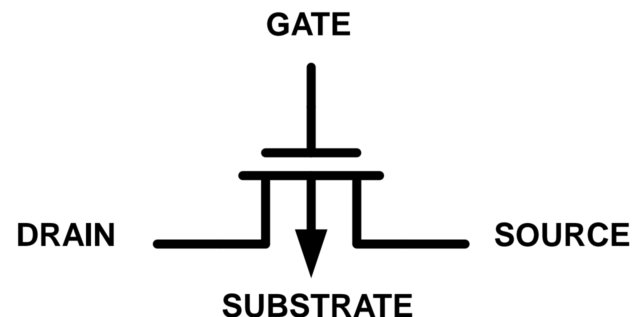
symbol



PMOS

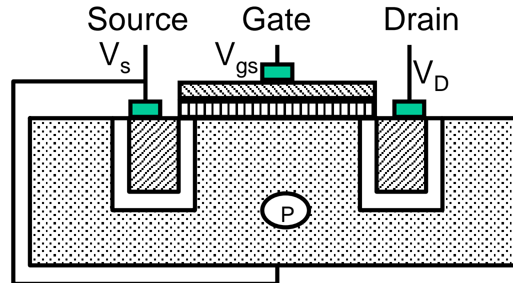


symbol

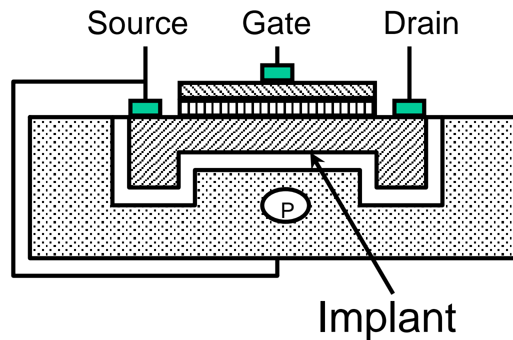


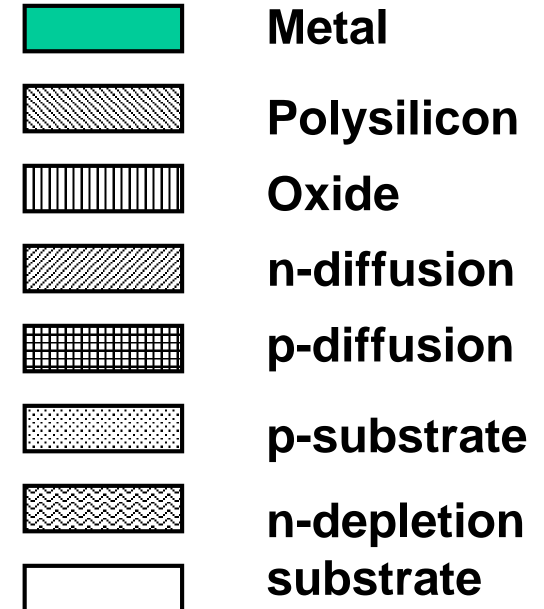
MOS Transistors (Cont.)

-Enhancement NMOS

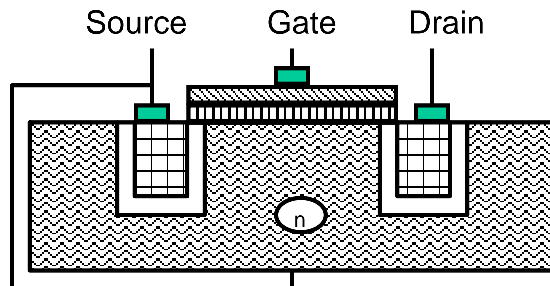


-Depletion NMOS

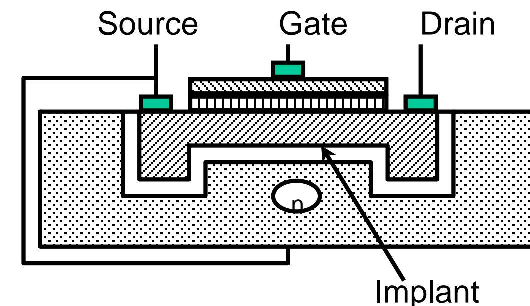




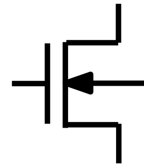
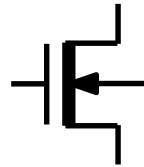
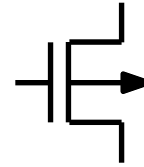
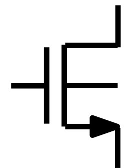
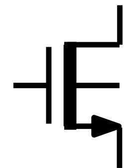
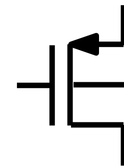
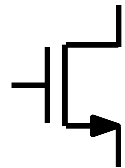
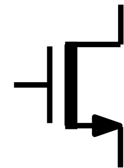
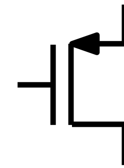
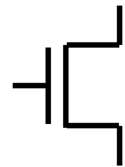
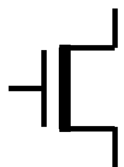
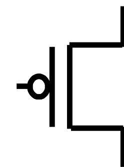
-Enhancement PMOS



-Depletion PMOS



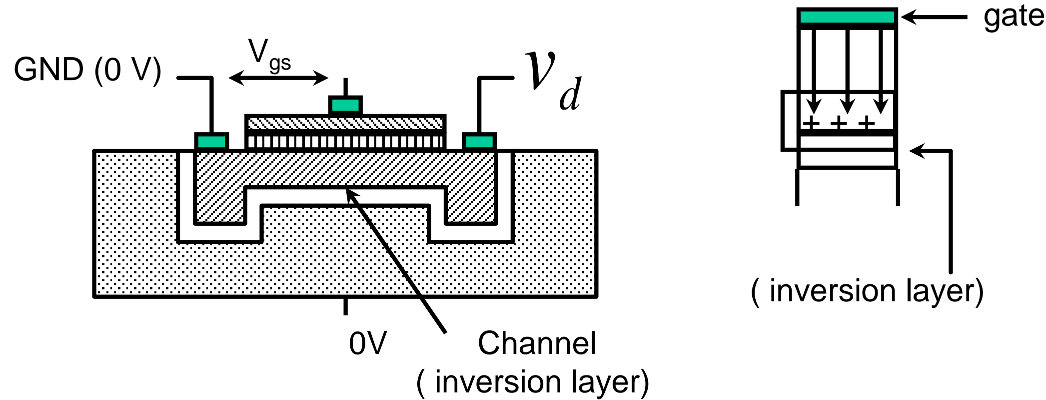
MOS Transistor Symbol (Cont.)

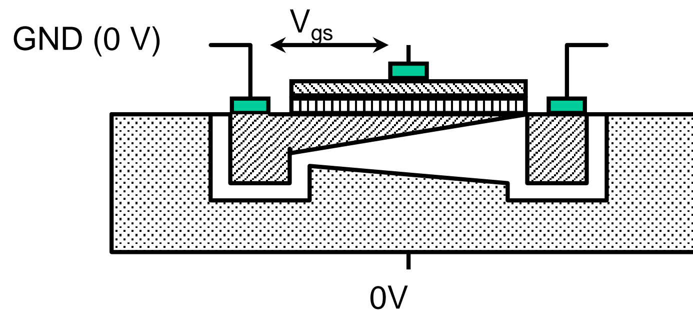
nMOS enhancement	nMOS depletion	pMOS enhancement

MOS Transistor Operation

- Example : nMOS
  - $V_{gs} > V_t$, $V_{ds} = 0$ (linear region)

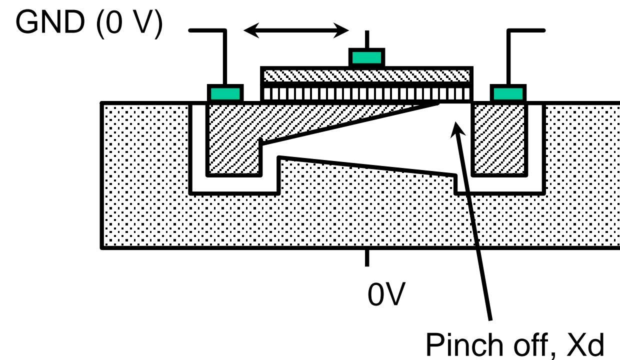


  - $V_{gs} > V_t$, $V_{ds} = V_{gs}-V_t$

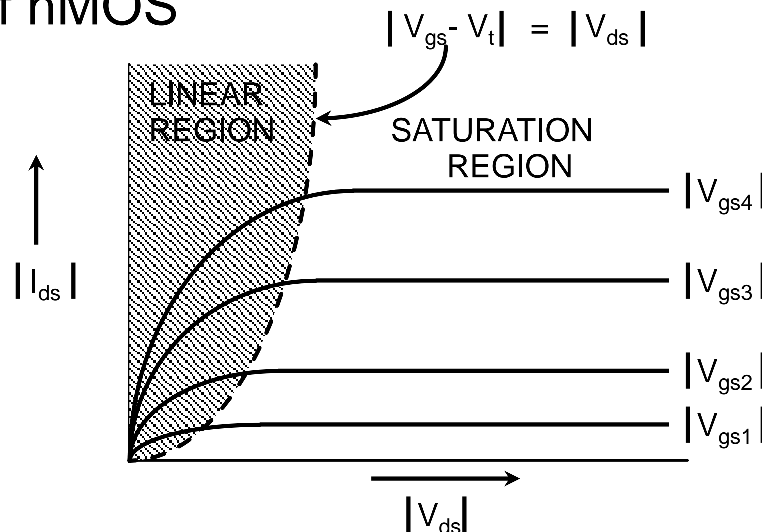


MOS Transistor Operation (Cont.)

- Example : nMOS
  - $V_{gs} > V_t$, $V_{ds} > V_{gs}-V_t$ (saturation region)



- I-V characteristic of nMOS



Large Signal Behavior of MOSFETs

- Threshold voltage

$$V_t = V_{t0} + \frac{\sqrt{2 q \varepsilon_{SiO_2} N_A}}{C_{ox}} \left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$$

$$= V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)$$

$$\text{where } \gamma = \frac{\sqrt{2 q \varepsilon_{SiO_2} N_A}}{C_{ox}} \quad \text{and } C_{OX} = \frac{k_{ox}\,\varepsilon_0}{t_{ox}} = \frac{\varepsilon_{ox}}{t_{ox}}$$

- Large-Signal I-V

$$I_{DS} = \frac{\mu C_{ox} W}{2L}\left(V_{GS} - V_t\right)^2 = \frac{kW}{2L}\left(V_{GS} - V_t\right)^2$$

If depletion-layer width X_d is considered L_{eff} = L-X_d

$$\Rightarrow I_{DS} = \frac{kW}{2L_{eff}}\left(V_{GS} - V_t\right)^2$$

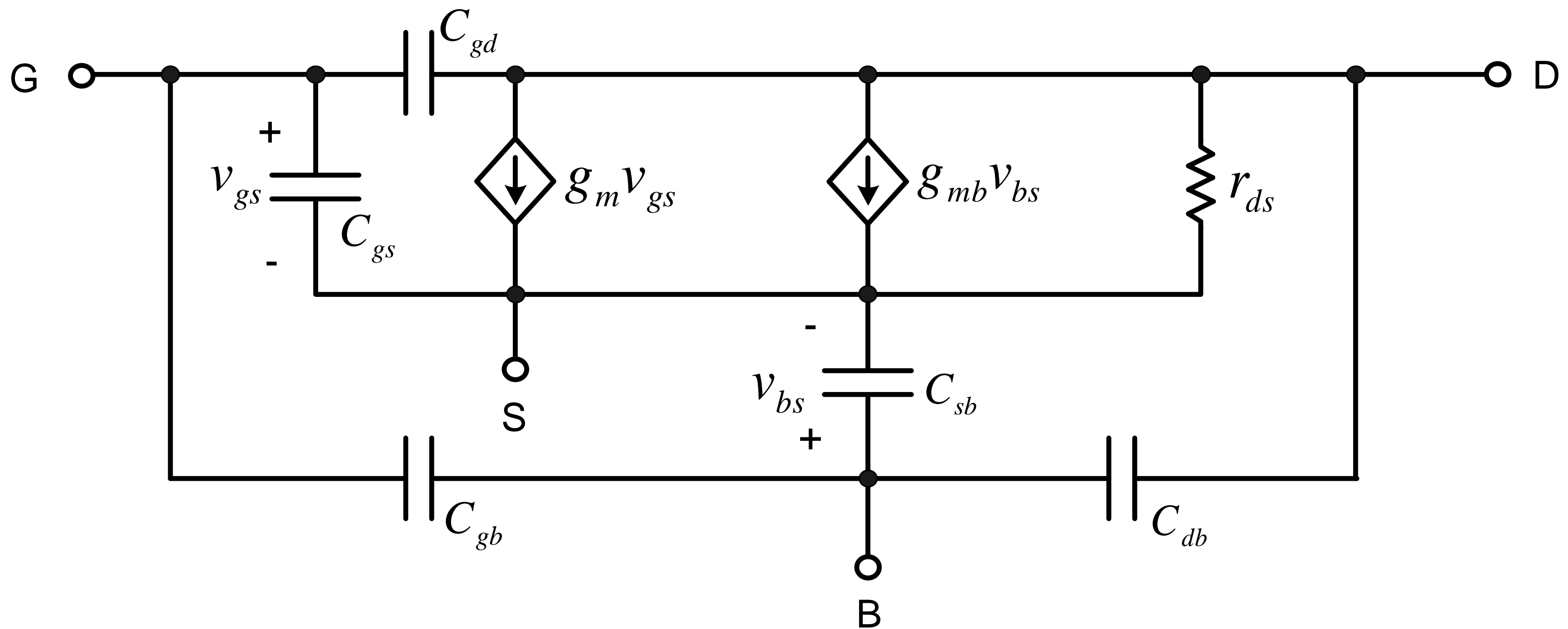
- Channel length modulation

$$\frac{\partial I_{DS}}{\partial V_{DS}} = -\frac{kW}{2L_{eff}^2}\left(V_{GS} - V_t\right)^2 \frac{dL_{eff}}{dV_{DS}} = \frac{I_{DS}\,dx_d}{L_{eff}\,dV_{DS}}$$

Let $\left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1} = r_{ds} = \frac{1}{\lambda I_{DS}} = \frac{V_A}{I_{DS}} \Rightarrow \lambda = \frac{1}{V_A} = \frac{1}{L_{eff}}\left(\frac{dx_d}{dV_{DS}}\right) \Rightarrow I_{DS} = \frac{kW}{2L}\left(V_{GS} - V_t\right)^2\left(1 + \lambda V_{DS}\right)$

Small Signal Model of MOSFETs in Saturation

- Equivalent circuit model



Small Signal Model of MOSFETs in Saturation (Cont.)

- $$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = k'\frac{W}{L}(V_{GS} - V_t) = \sqrt{2k\frac{W}{L}I_{DS}}$$ $$\lambda V_{DS} << 1$$
- $$g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} = k\frac{W}{L}(V_{GS} - V_t)\frac{\partial V_t}{\partial V_{BS}} = \chi g_m$$ $$\frac{\partial V_t}{\partial V_{BS}} = \frac{\partial\left(V_{to} + \gamma\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right)}{\partial V_{BS}} = \frac{-\gamma}{2\sqrt{2\phi_f + V_{BS}}} = \chi$$
- $$r_{ds} = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1} = \frac{L_{eff}}{I_{DS}}\left(\frac{dX_d}{dV_{DS}}\right)^{-1} = \frac{1}{\lambda I_{DS}} = \frac{V_A}{I_{DS}}$$
- $$C_{sb} = \frac{C_{sb0}}{\left(1 + \frac{V_{SB}}{\varphi_0}\right)^{1/2}}$$
- $$C_{db} = \frac{C_{db0}}{\left(1 + \frac{V_{DB}}{\varphi_0}\right)^{1/2}}$$
- $$C_{gs} = \frac{\partial Q_T}{\partial V_{GS}} \approx \frac{2}{3}WLC_{OX}$$

$$f_t = \frac{g_m}{2\pi C_{gs}} = \frac{1}{2\pi}\frac{K\frac{W}{L}(V_{GS} - V_t)}{\frac{2}{3}WLC_{ox}}$$

$$\omega_t = 2\pi f_t = \frac{3\mu}{2L^2}(V_{GS} - V_t)$$

- Derivation of C_{gs}
  - Total charge stored in the channel Q_T

$$Q_T = -WC_{ox}\int_0^L [V_{GS} - V(y) - V_t]\,dy = -\int_0^{V_{GS}-V_t}\frac{W^2C_{ox}^2\mu}{I_D}(V_{GS} - V - V_t)^2 dV$$

$$= \frac{2}{3}WLC_{ox}(V_{GS} - V_t)$$

$$C_{gs} = \frac{\partial Q_T}{\partial V_{GS}} = \frac{2}{3}WLC_{ox}$$

Example—Small Signal Model

- Derive the complete small-signal model for an NMOS transistor with I_{DS}=100μA, V_{SB}=0.15V, V_{DS}=0.6V. Device parameters are $2\phi_f = 0.65$, W=2.5 μm, L=45 nm, γ= 0.45$V^{1/2}$, $\mu_n C_{ox}$ = 280μA/V^2 , λ = 2.22V^{-1}, t_{ox} = 1.2 nm, Ψ_0 = 0.69 V, $C_{sb0} = C_{db0}$ = 1.125 fF. Overlap capacitance from gate to source and gate to drain is 1.25 fF. Assume C_{gb} =5fF.

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \sqrt{2\times 280\times 10^{-6}\times\frac{2.5}{0.045}\times 100\times 10^{-6}}\ A/V = 1.76\ mA/V$$

$$g_{mb} = \gamma\sqrt{\frac{\mu_n C_{ox}\frac{W}{L}I_D}{2(2\phi_f + V_{SB})}} = 0.45\sqrt{\frac{280\times 10^{-6}\times\frac{2.5}{0.045}\times 100\times 10^{-6}}{2\times(0.65+0.15)}}\ A/V = 443\ \mu A/V$$

$$r_{ds} = \frac{1}{\lambda I_{DS}} = \frac{1}{2.22\times 100\times 10^{-6}} = 22.2k\Omega$$

Example—Small Signal Model (Cont.)

- With V_{SB}=0.15V,we find $C_{sb} = \frac{C_{sb0}}{\left(1+\frac{V_{SB}}{\psi_0}\right)^{1/2}} = \frac{1.125}{\left(1+\frac{0.15}{0.69}\right)^{1/2}} \text{fF} = 1\text{fF}$

- The voltage from drain to body is $V_{DB} = V_{DS} + V_{SB} = 0.75\,\text{V}$

  Hence ,$C_{db} = \frac{C_{db0}}{\left(1+\frac{V_{DB}}{\psi_0}\right)^{1/2}} = \frac{1.125}{\left(1+\frac{0.75}{0.69}\right)^{1/2}} \text{fF} = 1.85\text{fF}$

- The oxide capacitance per unit area is

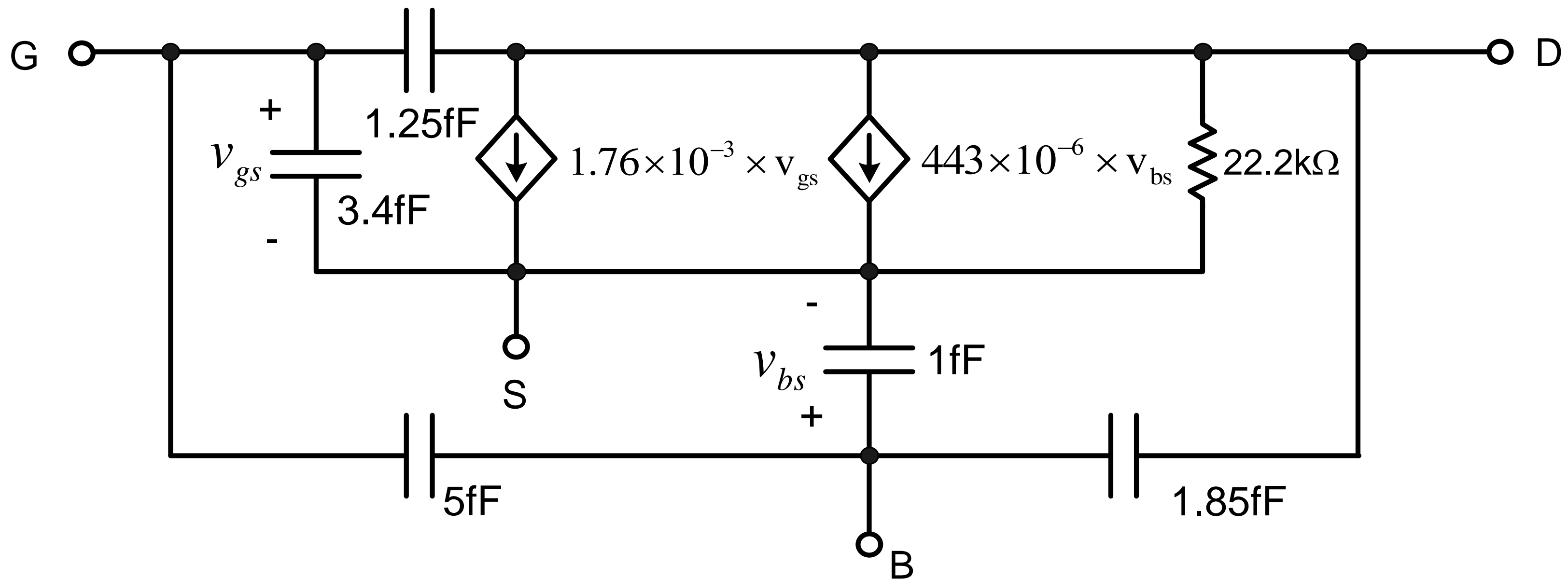
$$C_{ox} = \frac{\varepsilon_r \varepsilon_{SiO_2}}{t_{ox}} = \frac{3.9 \times 8.854 \times 10^{-14}\ \text{F}/\text{cm}}{1.2 \times 10^{-9}\,\text{m}} \approx 28.7\ \text{fF}/(\mu\text{m})^2$$

- The intrinsic portion of the gate source capacitance is

$$C_{gs} = \frac{2}{3} \times 2.5 \times 0.045 \times 28.7\text{fF} \approx 2.15\text{fF}$$

Example—Small Signal Model (Cont.)

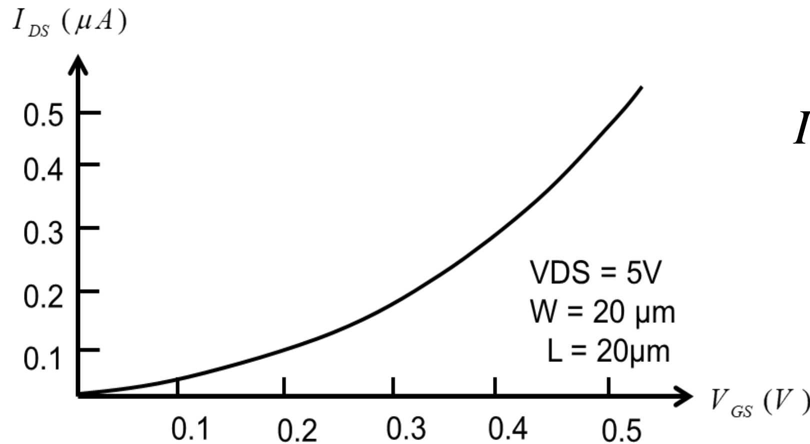
- The addition of overlap capacitance gives $C_{gs} = 3.4$ fF
- Gate-drain capacitance is overlap capacitance $C_{gd} = 1.25$ fF
- The complete small-signal equivalent circuit is shown below



- The f_T of the device can be calculated with $C_{gb} = 5$fF giving

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs} + C_{gd} + C_{gb}} = \frac{1}{2\pi}\frac{1.76 \times 10^{-3}}{(3.4 + 1.25 + 5) \times 10^{-15}} \cong 29 \text{ GHz}$$

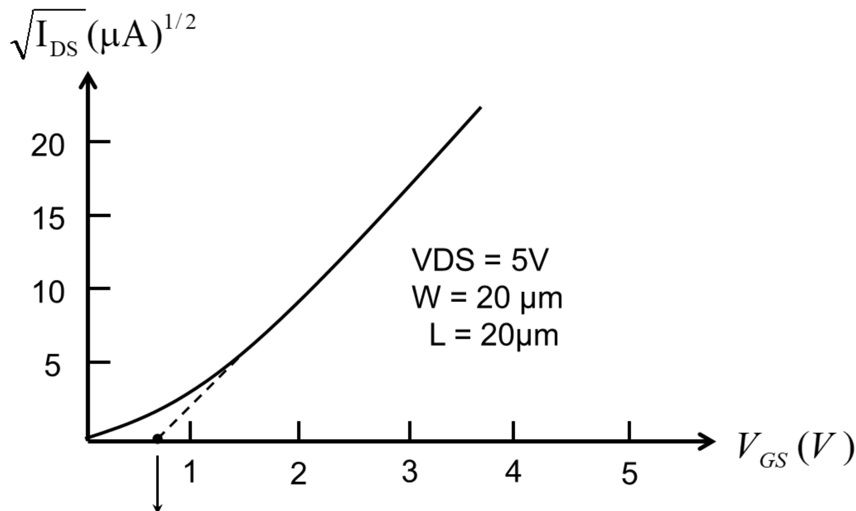
Subthreshold Conduction in MOSFETs



$$I_{DS} = k_x \frac{W}{L} \exp^{\frac{V_{eff}}{nVt}} \left(1 - \exp^{\frac{-V_{DS}}{nVt}} \right)$$

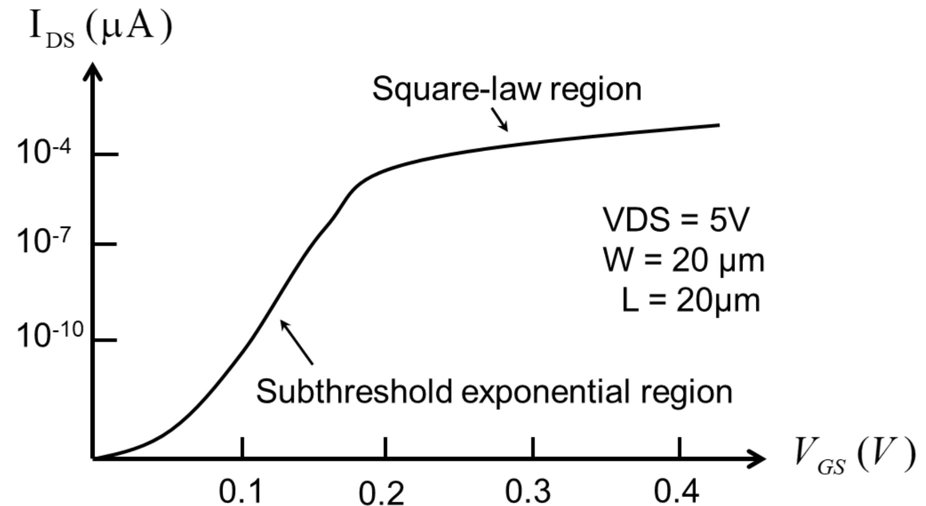
where k_x depends on process parameters

$n \approx 1.5$



Plot on linear scales as $\sqrt{I_{DS}}$ versus V_{GS}

→ Show square-law characteristic



Plot on log-linear scales

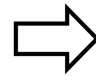
→ Show exponential characteristic in the subthreshold region

Mobility Degradation

- Large lateral electric fields accelerate carriers up to a maximum velocity
- Larger vertical electric fields → effective channel depth ↓ → collisions ↑
- These effects can be modeled by an effective carrier mobility

$$\mu_{n,eff} \approx \frac{\mu_n}{[1+(\theta V_{eff})^m]^{1/m}}$$

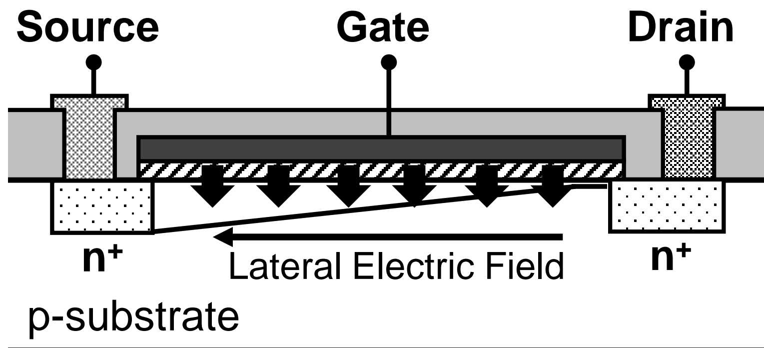
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{eff}^2\left(\frac{1}{[1+(\theta V_{eff})^m]^{1/m}}\right)$$

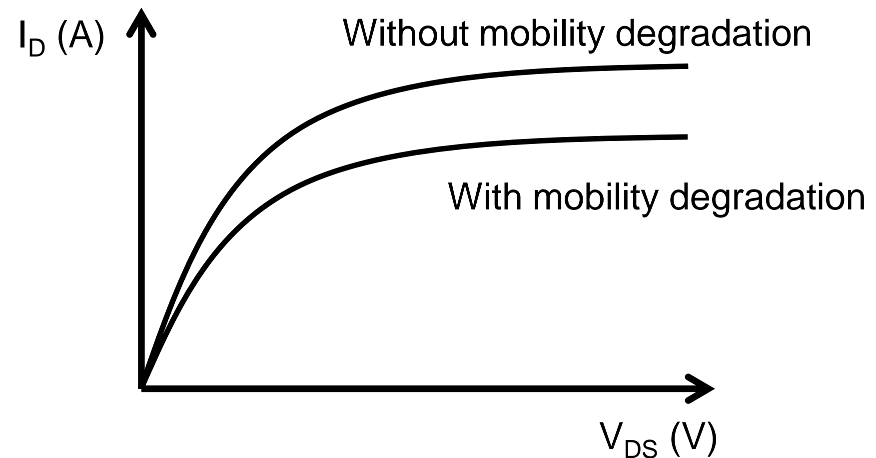


$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{eff}^{\alpha}\ ,\ \alpha < 2$$

where θ and m are device parameters

This effect can also expressed as α-law model from curve-fitting





Substrate Current Flow in MOSFETs

$$I_{DB} = k_1\left(V_{DS} - V_{DS(sat)}\right)I_{DS}\exp[-\frac{k2}{\left(V_{DS} - V_{DS(sat)}\right)}]$$

where k_1 and k_2 are process-dependent parameters and V_{DSsat} is the value of V_{DS} where the drain characteristics enter the saturation region

$$g_{db} = \frac{\partial I_{DB}}{\partial V_{DB}} = \frac{k_2 I_{DB}}{\left(V_{DS} - V_{DS(sat)}\right)^2}$$

Example (1/2)

- Calculate $r_{db} = 1/g_{db}$ for $V_{DS} = 2$ V and 4 V, and compare with the device r_{ds}.

  Assume I_{DS} = 100μA, λ = 0.45 V^{-1}, $V_{DS(sat)}$ = 0.3 V, K1 = 5 V^{-1}, and K2 = 30 V.

For V_{DS} = 2 V, we have

$$I_{DB} = 5 \times \ 1.7 \times 100 \times 10^{-6} \times \exp\left(-\frac{30}{1.7}\right) = 1.8 \times 10^{-11} \ \text{A}$$

$$g_{db} = \frac{30 \times 1.8 \times 10^{-11}}{1.7^2} = 1.9 \times 10^{-10} \ \frac{\text{A}}{\text{V}}$$

and thus

$$r_{db} = \frac{1}{g_{db}} = 5.3 \times 10^9 \ \Omega = 5.3 \ \text{G}\Omega$$

Example (2/2)

This result is negligibly large compared with

$$r_{ds} = \frac{1}{\lambda I_D} = \frac{1}{0.45 \times 100 \times 10^{-6}} = 22.2\ \text{k}\Omega$$

However, for $V_{DS} =$ 4 V

$$\text{I}_{\text{DB}} = 5 \times 3.7 \times 100 \times 10^{-6} \times \exp\left(-\frac{30}{3.7}\right) = 5.6 \times 10^{-7}\ \text{A}$$

The substrate leakage current is now about 0.5% of the drain current. We find

$$\text{g}_{\text{db}} = \frac{30 \times 5.6 \times 10^{-7}}{3.7^2} = 1.2 \times 10^{-6}\ \frac{\text{A}}{\text{V}}$$

and thus

$$\text{r}_{\text{db}} = \frac{1}{\text{g}_{\text{db}}} = 8.33 \times 10^5\ \Omega = 833\ \text{k}\Omega$$

This parasitic resistor is now comparable to r_{ds} and can have a dominant effect on high-output-impedance MOS current mirrors.

Summary of MOSFET Parameters

- Large-Signal Operation

Quantity	Formula
Drain current (saturation region)	$I_{ds} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{gs} - V_t)^2(1 + \lambda V_{ds})$
Drain current (triode region)	$I_{ds} = \frac{\mu C_{ox}}{2}\frac{W}{L}[2(V_{gs} - V_t)V_{ds} - V_{ds}{}^2]$
Threshold voltage	$V_t = V_{t0} + \gamma[\sqrt{2\varphi_f - V_{sb}} - \sqrt{2\varphi_f}]$
Threshold voltage parameter	$\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon N_A}$
Oxide capacitance	$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 3.45\ fF/\mu m^2 \text{ for } t_{ox} = 100\ \mathring{A}$

Summary of MOSFET Parameters

- Large-Signal Operation

Quantity	Formula
Top-gate transconductance	$g_m = \mu C_{ox} \frac{W}{L}(V_{GS} - V_t) = \sqrt{2I_{DS}\mu C_{ox}\frac{W}{L}}$
Transconductance-to-current ratio	$\frac{g_m}{I_{DS}} = \frac{2}{V_{GS} - V_t}$
Body-effect transconductance	$g_{mb} = \frac{\gamma}{2\sqrt{2\varphi_f + V_{SB}}} g_m = \chi g_m$
Channel-length modulation parameter	$\lambda = \frac{1}{V_A} = \frac{1}{V_{eff}}\frac{dX_d}{dV_{DS}}$
Output resistance	$r_{ds} = \frac{1}{\lambda I_{DS}} = \frac{L_{eff}}{I_{DS}}\left(\frac{dX_d}{dV_{DS}}\right)^{-1}$

Summary of MOSFET Parameters

Quantity	Formula
Effective channel length	$L_{eff} = L_{drwn} - 2L_d - X_d$
Maximum gain	$g_m r_{ds} = \frac{1}{\lambda}\frac{2}{V_{GS} - V_t} = \frac{2V_A}{V_{GS} - V_t}$
Source-body depletion capacitance	$C_{sb} = \frac{C_{sb0}}{\left(1 + \frac{V_{SB}}{\psi_0}\right)^{0.5}}$
Drain-body depletion capacitance	$C_{db} = \frac{C_{db0}}{\left(1 + \frac{V_{DB}}{\psi_0}\right)^{0.5}}$
Gate-source capacitance	$C_{gs} = \frac{2}{3} WLC_{ox}$
Transition frequency	$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd} + C_{gb}\right)}$

SPICE MOSFET Model Parameters of A Typical NMOS Process (MOSIS)

Parameter (Level 2 model)	Enhancement	Depletion	Units
VTO	1.14	-3.79	V
KP	37.3	32.8	$\mu A/V^2$
GAMMA	0.629	0.372	$V^{1/2}$
PHI	0.6	0.6	V
LAMBDA	3.1E-2	1.00E-6	V^{-1}
CGSO	1.60E-4	1.60E-4	fF/μ width
CGDO	1.60E-4	1.60E-4	fF/μ width
CGBO	1.70E-4	1.70E-4	fF/μ width
RSH	25.4	25.4	$\Omega/\square$
CJ	1.1E-4	1.1E-4	pF/μ^2
MJ	0.5	0.5	
CJSW	5.0E-4	5.0E-4	pF/μ^2 perimeter
MJSW	0.33	0.33	
TOX	544	544	Å

SPICE MOSFET Model Parameters of A Typical NMOS Process (MOSIS) (Cont.)

(Level 2 model)	Enhancement	Depletion	Units
NSUB	2.09E15	1.0E16	$1/cm^2$
NSS	0	0	$1/cm^3$
NFS	1.90E12	4.3E12	$1/cm^2$
TPG	1	1	
XJ	1.31	0.6	
LD	0.826	1.016	μ
UO	300	900	μ
UCRIT	1.0E6	0.805E6	$cm^2/(v \cdot s)$
UEXP	1.001E-3	1.001E-3	V/cm
VMAX	1.0E5	6.75E5	m/s
NEFF	1.001E-2	1.001E-2	
DELTA	1.16	2.80	

- The SPICE parameters: Empirical parameters
  - Fitting measured device characteristics to the mathematical equations
  - Using a numerical optimization algorithm
- This approach gives good fit to the model but causes a deviation from the typical parameters.
- Parameter relationships may not be self-consistent with some of the fundamental relationships.

*Please refer to the chapters about SPICE model in the HSPICE document suggested in assignment 1

Appendix

- Resistance Estimation
- Capacitance Estimation
- Inductance Estimation

Resistance Estimation

- Sheet Resistance
  - $R=\rho L/A=\rho L/tW= R_{\square}L/W$
  - $R_{\square}=\rho/t$

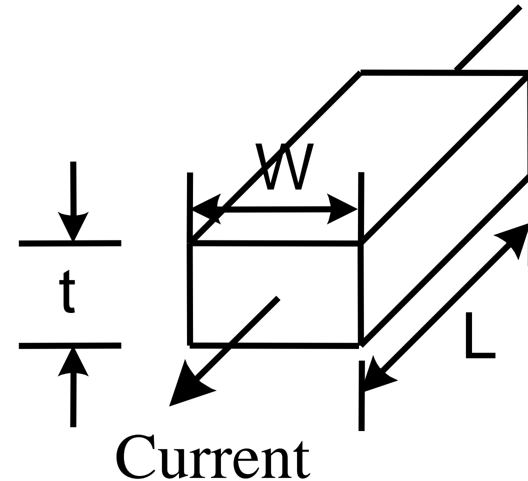
ρ : resistivity

t : thickness

L : conductor length

W : conductor width

$R_{\square}$: sheet resistance (ohm/square, $\Omega/\square$)



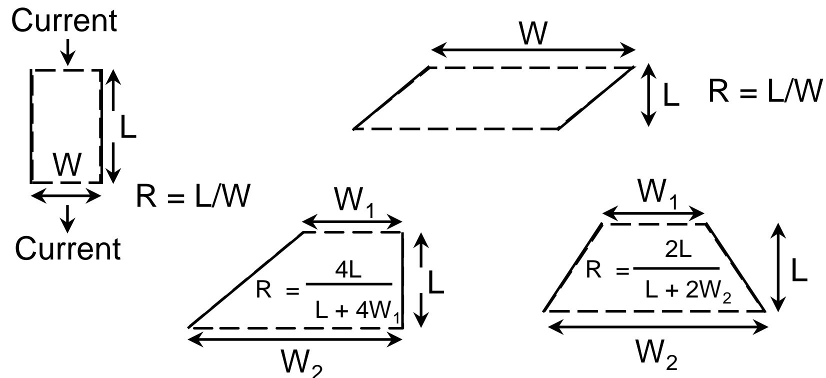
Resistance Estimation (cont.)

- Typical sheet resistance for conductors

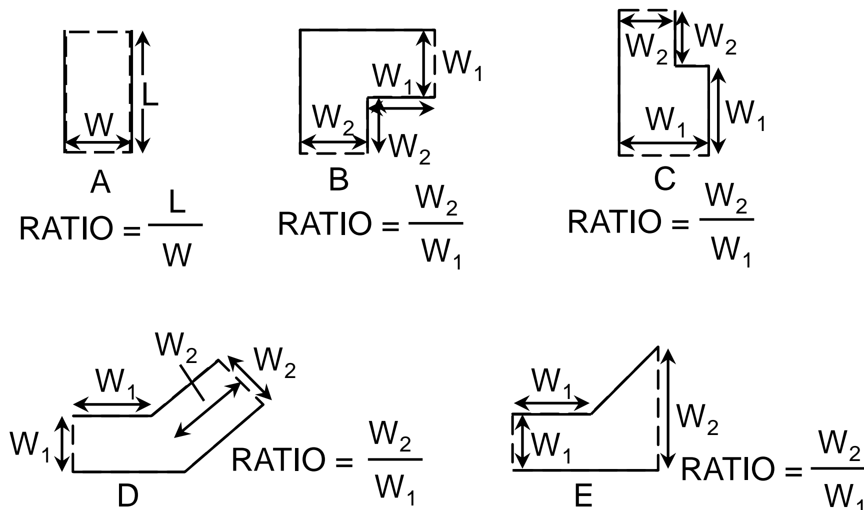
Material	Min.	Typical	Max.
Intermatal (metal1-metal2)	0.05	0.07	0.1
Top-metal(metal3)	0.03	0.04	0.05
Polysilicon	15	20	30
Silicide	2	3	6
Diffusion(n^+, p^+)	10	25	100
Silicided diffusion	2	4	10
N-well	1K	2K	5K

Resistance Estimation of Nonrectangular Shapes

- Direct estimation



- Table-assisted estimation



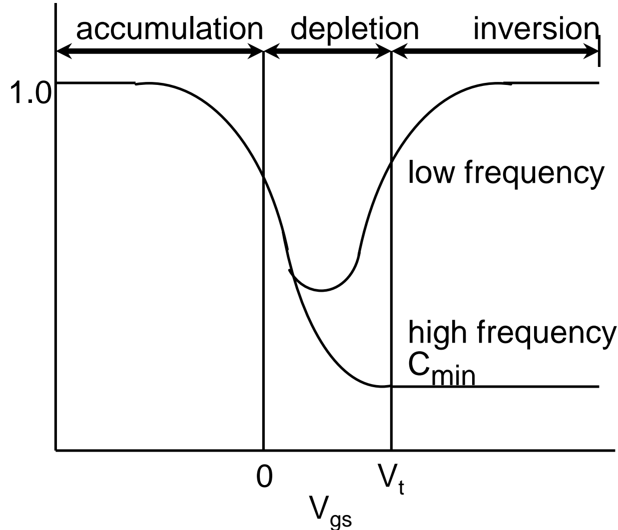
Shape	Ratio	Resistance
A	1	1
A	5	5
B	5	5
B	1	2.5
B	2	2.55
B	3	2.66
C	1.5	2.1
C	2	2.25
C	3	2.5
C	4	2.65
D	1	2.2
D	1.5	2.3
D	2	2.3
D	3	2.6
E	1.5	1.45
E	2	1.8
E	3	2.3
E	4	2.65

Contact and Via Resistance

- Proportional to the area of the contact
  - e.g. feature size↓ =>Rcontact↑
- 0.25Ω ~ a few tens of Ωs
- Multiple contacts to obtain low-resistance interlayer connections

MOS-Capacitor Characteristics

- C-V plot



Three regions in the plot

(i)Accumulation region

(ii)Depletion region

(iii)Inversion region

- Accumulation region

$$C_o = \frac{\varepsilon_{SiO_2}\varepsilon_o}{t_{ox}} A = C_{ox} \bullet A$$

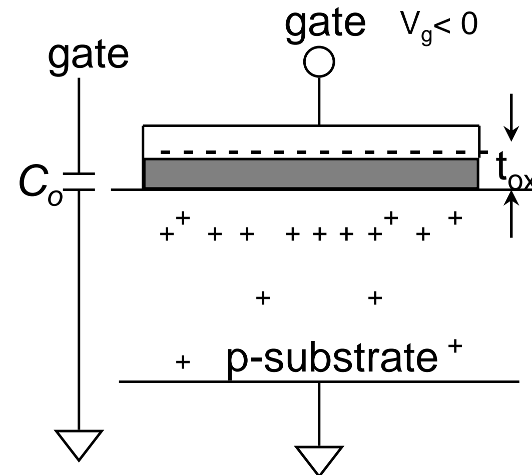
C_o : *gate* capacitance

ε_{SiO_2} : dielectric constant of SiO_2 (= 3.9)

ε_o : permittivity of free space

A : gate area

$$C_{ox} = \frac{\varepsilon_{SiO_2}\varepsilon_o}{t_{ox}}$$: gate capacitance per unit area



MOS-Capacitor Characteristics (cont.)

- Depletion region

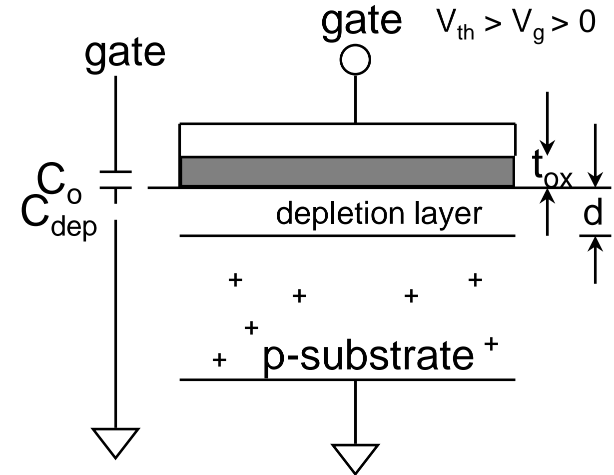
$$C_{dep} = \frac{\varepsilon_{Si}\varepsilon_o}{d} A = C_{ox}$$

d : depletion layer depth

ε_{Si} : dielectric constant of Si(=12)

$$C_{gb} = \frac{C_o C_{dep}}{C_o + C_{dep}}$$: gate capacitance per unit area

Where C_o is low frequency capacitance between gate and surface



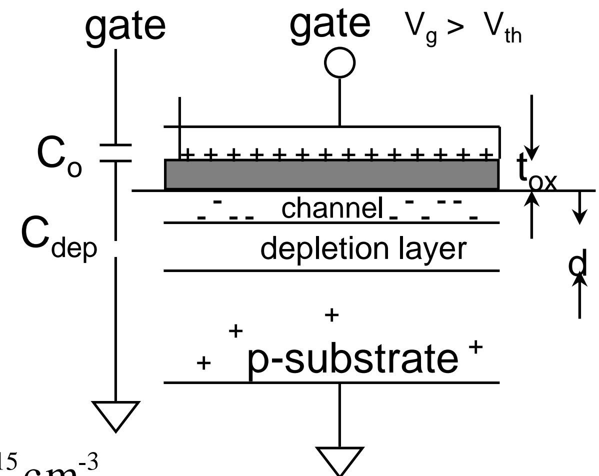
- Inversion region

$$C_{gb} = \begin{cases} C_o : \text{static (i.e. low frequency, < 100Hz)} \\ \dfrac{C_o C_{dep}}{C_o + C_{dep}} = C_{min} : \text{dynamic (i.e. high frequency)} \end{cases}$$

C_{min}

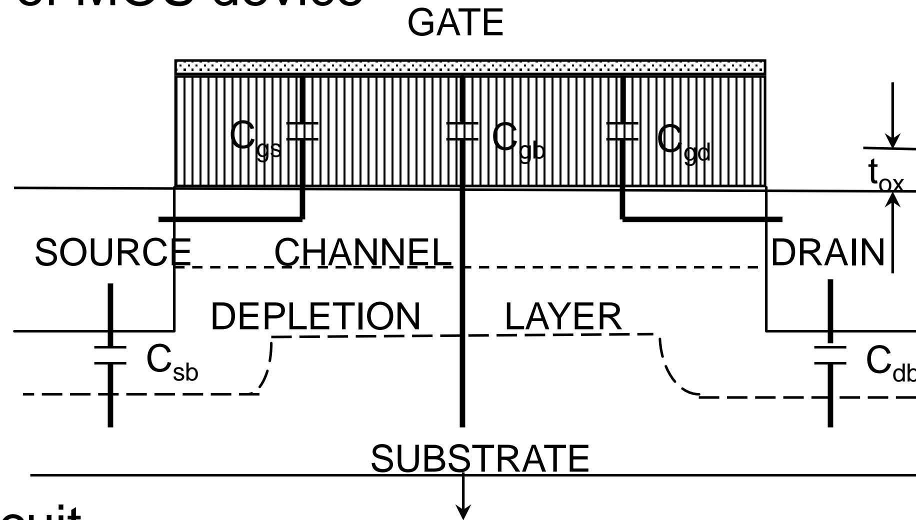
– C_{dep} depends on the depth of the depletoin region, i.e. depends on substrate doping density.

– For $t_{ox} = 100 \sim 200\,\mathring{A}$, C_{min}/C_o varies from $0.02 \sim 0.3$ for substrate doping density varies from $1\times10^{-14}\,cm^{-3}$ to $5\times10^{-15}\,cm^{-3}$

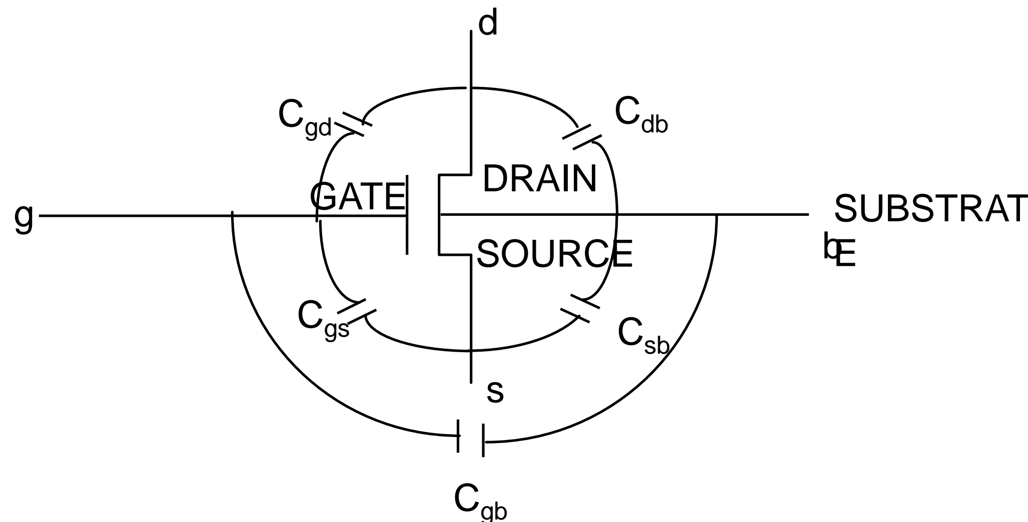


MOS Device Capacitance

- Cross section of MOS device



- Equivalent circuit



MOS Device Capacitance (cont.)

- Approximation of gate capacitance

—— Self-aligned process is assumed (i.e. overlap caps. are negligible)

Parameter	off	Non-saturated	Saturated
C_{gb}	$\frac{\varepsilon A}{t_{ox}}$	0	0
C_{gs}	0	$\frac{\varepsilon A}{2t_{ox}}$	$\frac{2\varepsilon A}{3t_{ox}}$
C_{gd}	0	$\frac{\varepsilon A}{2t_{ox}}$	0(finite for short channel devices)
$C_g=C_{gb}+C_{gs}+C_{gd}$	$\frac{\varepsilon A}{t_{ox}}$	$\frac{\varepsilon A}{t_{ox}}$	$\frac{2\varepsilon A}{3t_{ox}} \longrightarrow \frac{0.9\,\varepsilon A}{t_{ox}}$ (short channel)

Cgs,Cgd and Cox

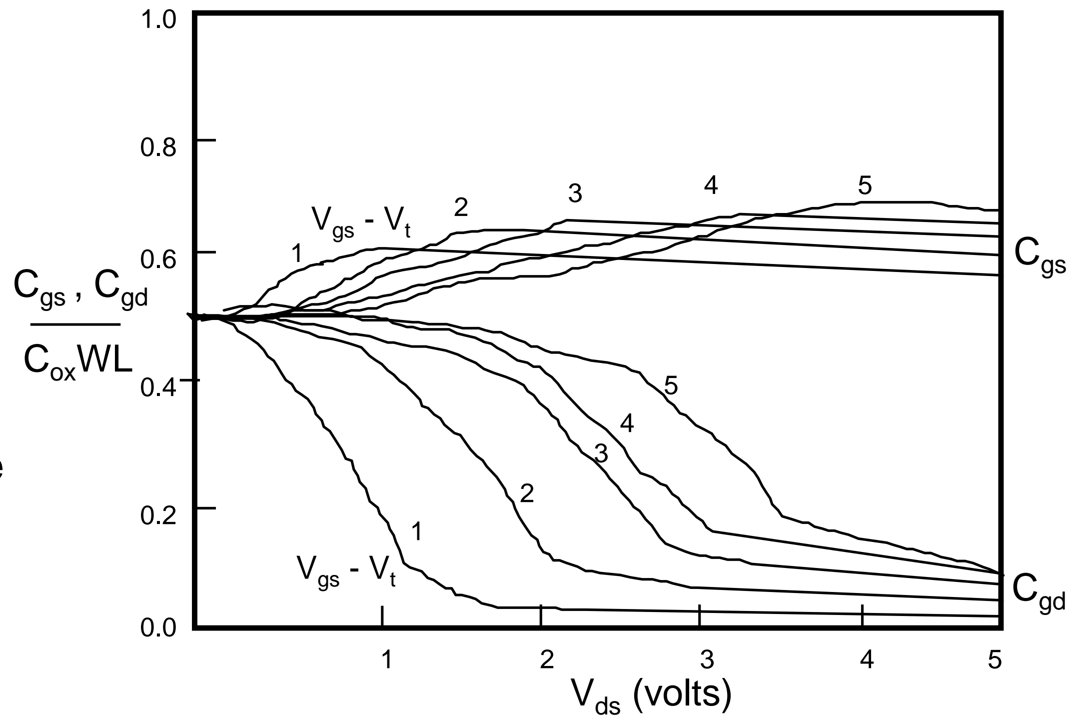
- Example 1: W=49.2μm, L=4.5μm (long channel)
  - ◆ C_{gs} and C_{gd}

large L

* large C_g & small C_{gd} (in saturation region)

$$\frac{C_{gd}}{C_g} \approx 0$$

(C_{gd} is due to channel side fringing fields between gate and drain.)



Cgs,Cgd and Cox (cont.)

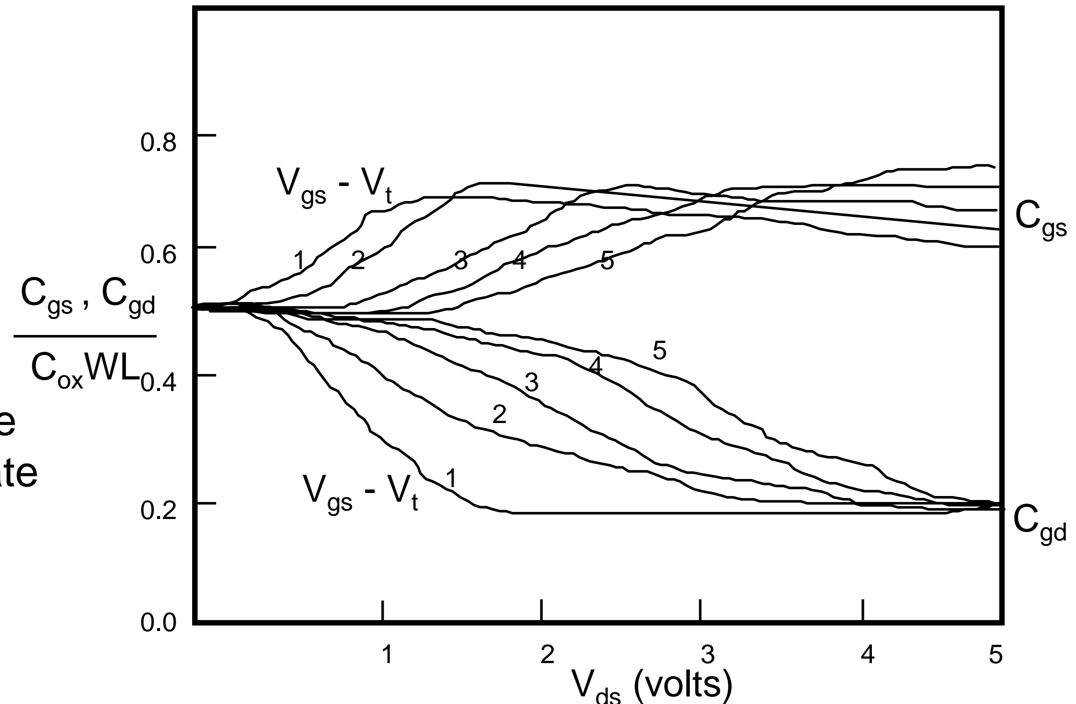
- Example 2: L=0.75μm (short channel)
  - C_{gs} and C_{gd}

small L

∗small C_g & small C_{gd} (in saturation region)

$$\frac{C_{gd}}{C_g} \approx 0.2$$

(C_{gd} is due to channel side fringing fields between gate and drain.)

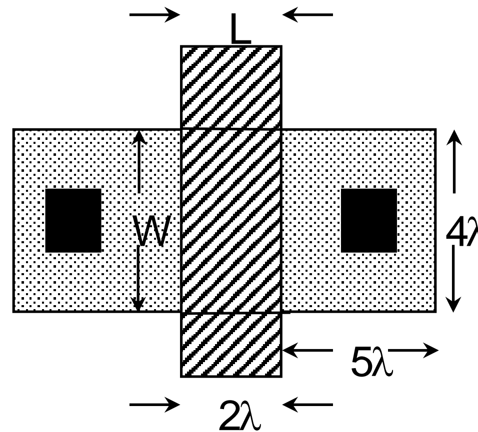


Cox, gate capacitance per unit area

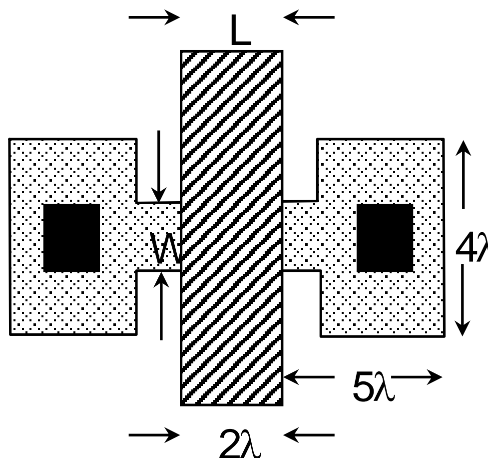
- $C_{ox} = \frac{\varepsilon_{SiO_2}\varepsilon_o}{t_{ox}} A$; where $\varepsilon_{SiO_2} = 3.9$ and $\varepsilon_o = 8.854 \times 10^{-14}$

  e.g. $t_{ox} = 350\,\mathring{A} \Rightarrow C_{ox} \approx 1 \times 10^{-3}\,pF/\mu F^2 = 1 fF/\mu f^2$

- Unit transistor
  - It is the same width as a metal-diffusion contact



- Minimum-size transistor



Diffusion Capacitance

- Area and periphery

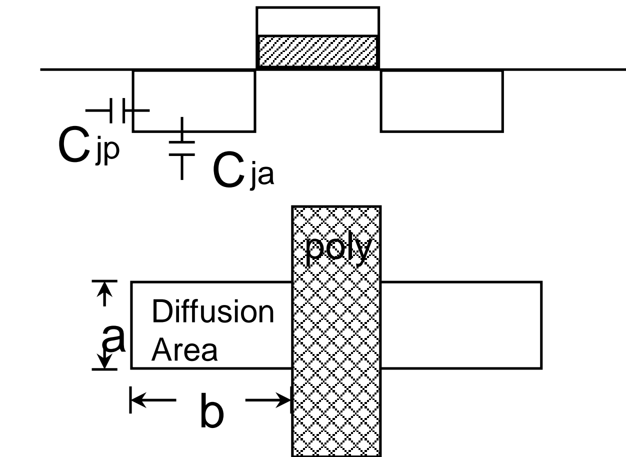
  Cd=Cja*(ab)+Cjp*(2a+2b)

  Cja: junction capacitance per μm^2

  Cjp: periphery capacitance per µm

  a: width of diffusion region

  b: length of diffusion region



- Typical value (1µm n-well process)

  Cja: $2*10^{-4}$pf/μm^2 (n+ diffusion)

  $5*10^{-4}$pf/μm^2 (p+ diffusion)

  Cjp: $4*10^{-4}$pf/μm^2 (n+ diffusion)

  $4*10^{-4}$pf/μm^2 (p+ diffusion)

- Voltage dependent

$$C_j(V_j) = C_{j0}\left(1 - \frac{V_j}{V_b}\right)^{-m}$$

V_j is junction voltage

V_b is built-in junction potential ~ 0.6V

C_{j0} is zero bias capacitance

$m = 0.3$(graded junction) ~

0.5(abrupt junction)

SPICE Modeling of MOS Capacitances

- SPICE example

```
.
M1 4 3 5 0 NFET W = 4U L = 1U AS = 15P AD = 15P PS = 11.5U PD = 11.5U
.
.
.MODEL NFET NMOS
+ TOX = 100E-8
+ CGBO = 200P CGSO = 600P CGDO = 600P
+ CJ = 200U CJSW = 400P MJ = 0.5 MJSW = 0.3 PB = 0.7
+ .....
.
.
```

node4 - drain
node3 - gate
node5 - source
node0 - substrate
channel width = 4μm
channel length = 1μm

TOX = 100 $\mathring{A}$
source area AS = 15μm^2
drain area AD = 15μm^2
source periphery PS = 11.5μm
drain periphery PD = 11.5μm

C_{gbo} occours due to the polysilicon extesion beyond the channel. $(200\times10^{-12}$ F/M$)$
C_{gso} and C_{gdo} represent the gate-to-source/drain capacitance due to overlap in the physical structure of the transistor. $(600\times10^{-12}$ F/M$)$

SPICE Modeling of MOS Capacitances (cont.)

- Capacitance

gate capacitance

$$C_{g(intrinsic)} = W \bullet L \bullet C_{OX} = 4 \times 1 \times 35 \times 10^{-4} PF = 0.014 PF$$

$$C_{g(extrinsic)} = (W \bullet C_{gs0}) + (W \bullet C_{gd0}) + (2L \bullet C_{gb0})$$

$$= 4 \times 6 \times 10^{-4} + 4 \times 6 \times 10^{-4} + 2 \times (1 \times 2 \times 10^{-4}) PF$$

$$= 0.0052 PF$$

$$C_{g(total)} = C_{g(intrinsic)} + C_{g(extrinsic)} \approx 0.02 PF$$

source and drain capacitance

$$C_j = \left(Area \bullet C_j \bullet \left(1 + \frac{VJ}{PB}\right)^{-MJ} \right) + \left(periphery \bullet CJSW \bullet \left(1 + \frac{VJ}{PB}\right)^{-MJSW} \right)$$

where

C_j = the zero-bias capacitance per junction area

CJSW = the zero-bias capacitance per junction periphery

MJ = the grading coefficient of the junction bottom

MJSW = the grading coefficient of the junction sidewall

VJ = the junction potential

PB = the built-in voltage (~ 0.4 - 0.8 volts)

Area = AS or AD, the area of the souce or drain

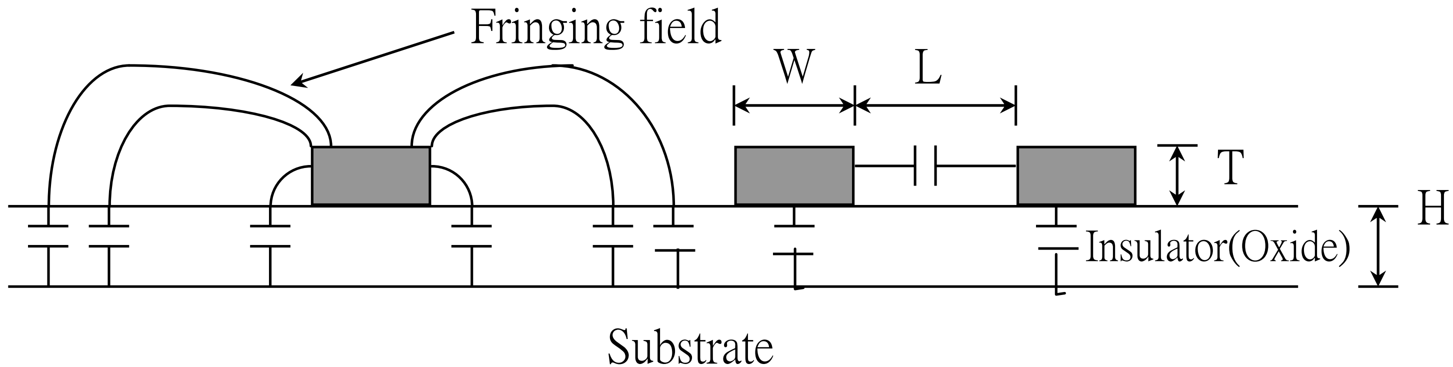
Periphery = PS or PD, the periphery of the source or drain

$C_{j(drain)} = 0.0043 PF$ (VJ = 2.5V is assumed)

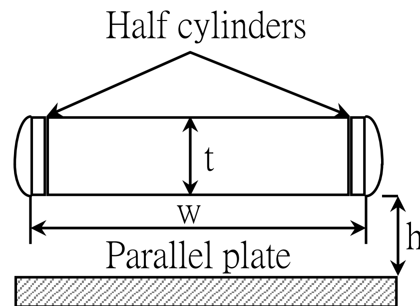
$C_{j(source)} = 0.0043 PF$ (VJ = 2.5V is assumed)

Routing Capacitance

- Single wire capacitance
  - Parallel-plate effect and fringing effect



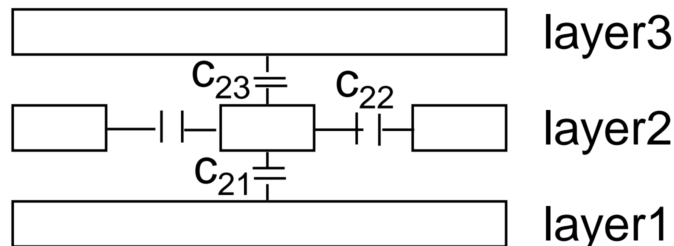
  - Accurate capacitance evaluation : use computer
  - Hand calculation : use simple model (less than 10% error)



$$C = \varepsilon\left[\left(\frac{w}{h}\right) + 0.77 + 1.06\left(\frac{w}{h}\right)^{0.25} + 1.06\left(\frac{t}{h}\right)^{0.5}\right]$$

Routing Capacitance (cont.)

- Multiple conductor capacitances
  - Three-layer example



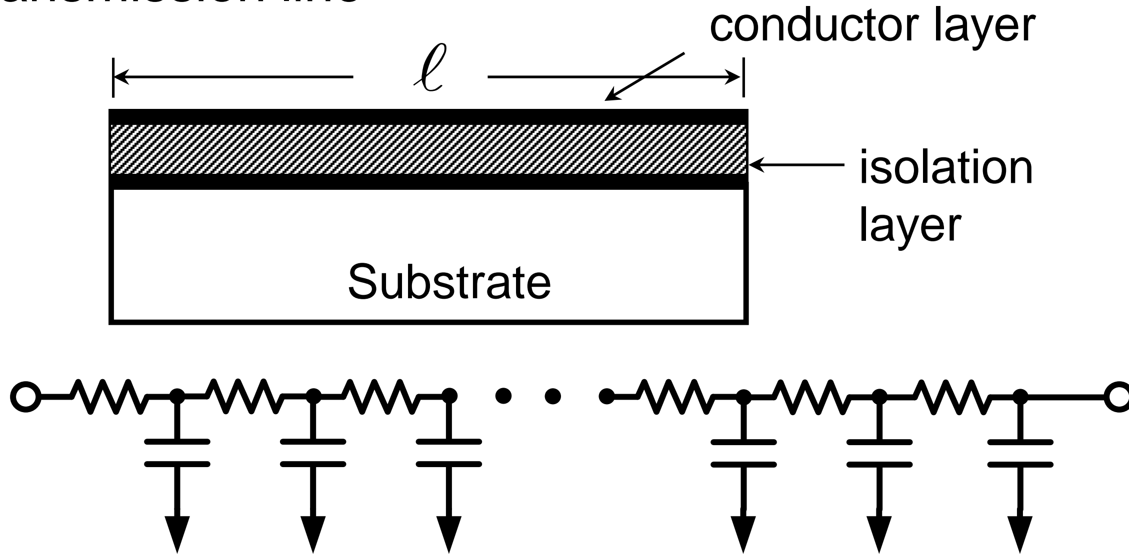
Capacitance calculation is very complex—refer to textbook

  - Typical dielectric and conductor thicknesses

Thin−oxide	200 Å	Metal1	6000 Å
Field−oxide	6000 Å	$M_1 - M_2$ oxide	6000 Å
Polysilicon	3000 Å	Metal2	12000 Å
M_1 −poly−oxide	6000 Å	Passivation	20000 Å

Distributed RC Effects

- Transmission line



- Delay time from one end to the other end

$$t \cong \frac{rc}{2} l^2$$

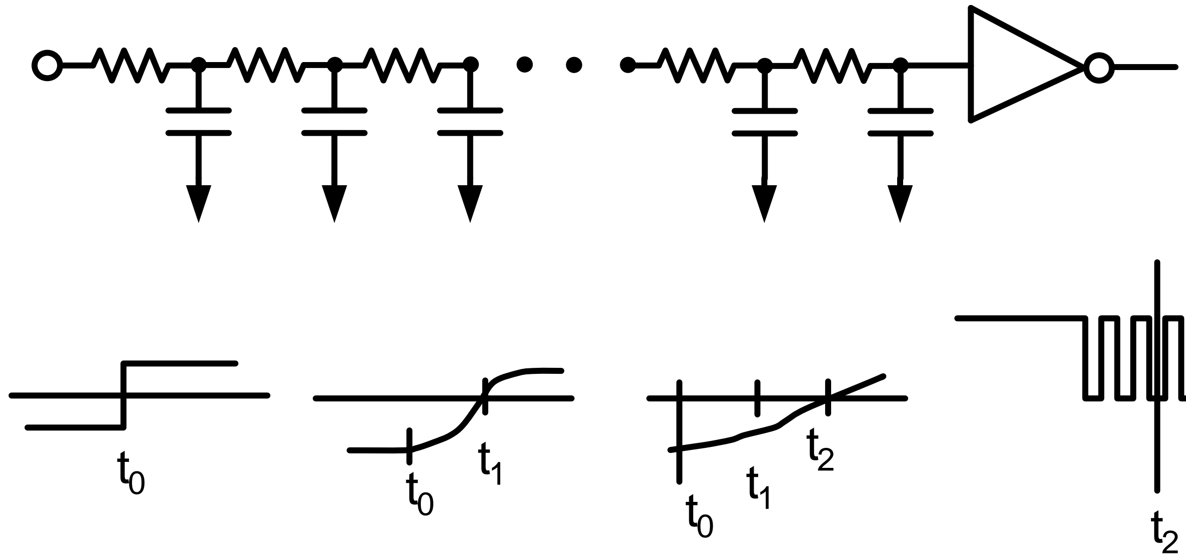
r : resistance per unit length

c : capacitance per unit length

l : length of the wire

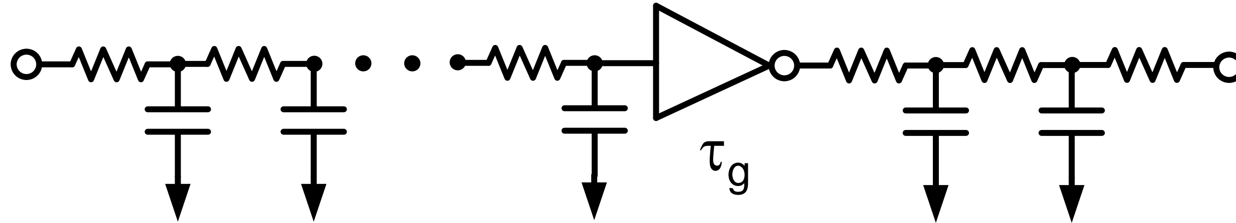
Distributed RC Effects (cont.)

- Disadvantages of long wire:
  - Long delay
  - Reduction in sensitivity to noise



Distributed RC Effects (cont.)

- Method to improve disadvantages mentioned previously



$$\text{delay} \approx \frac{rc}{2}\left(\frac{l}{2}\right)^2 + \tau_g + \frac{rc}{2}\left(\frac{l}{2}\right)^2$$

$$\approx \frac{rcl^2}{4} + \tau_g$$

$$\text{If } \left(\frac{rcl^2}{4}\right) < \tau_g, \text{ delay time is reduced}$$

$$\text{If } \left(\frac{rcl^2}{2}\right) >> \tau_g, \text{ more buffers should be used}$$

In actual design, if possible,

$$\frac{rcl^2}{2} << \tau_g \quad \Rightarrow \ell << \sqrt{\frac{2\tau_g}{rc}}$$

Distributed RC Effects (cont.)

- Transmission line effect is particularly severe in poly wire because of the relatively high resistance of this layer. Gate poly layer is the worst one because of its high capacitance to substrate.

- Strategies
  - Use metal line : small r
  - Use wider metal for signal distribution line
    - (e.g. clock distribution line) : small r, a tiny bit large C

Inductance

- On-chip inductance are normally small.
- Bond-wire inductance is larger.
- Inductance of bonding wires and the pins on packages

$$L = \frac{\mu}{2\pi} \ln\left(\frac{4h}{d}\right) \text{H/cm}$$

μ : the magnetic permeability of the wire

(typically 1.257×10^{-8} H/cm)

h : the height above the groundplane

d : the diameter of the wire

- Inductance of on-chip wires

$$L = \frac{\mu}{2\pi} \ln\left(\frac{8h}{w} + \frac{w}{4h}\right) \text{H/cm}$$

w : conductor width

h : the height above the substrate